Fluxul de operații

“CAE-CAD-CAM” pentru dezvoltarea modulelor electronice

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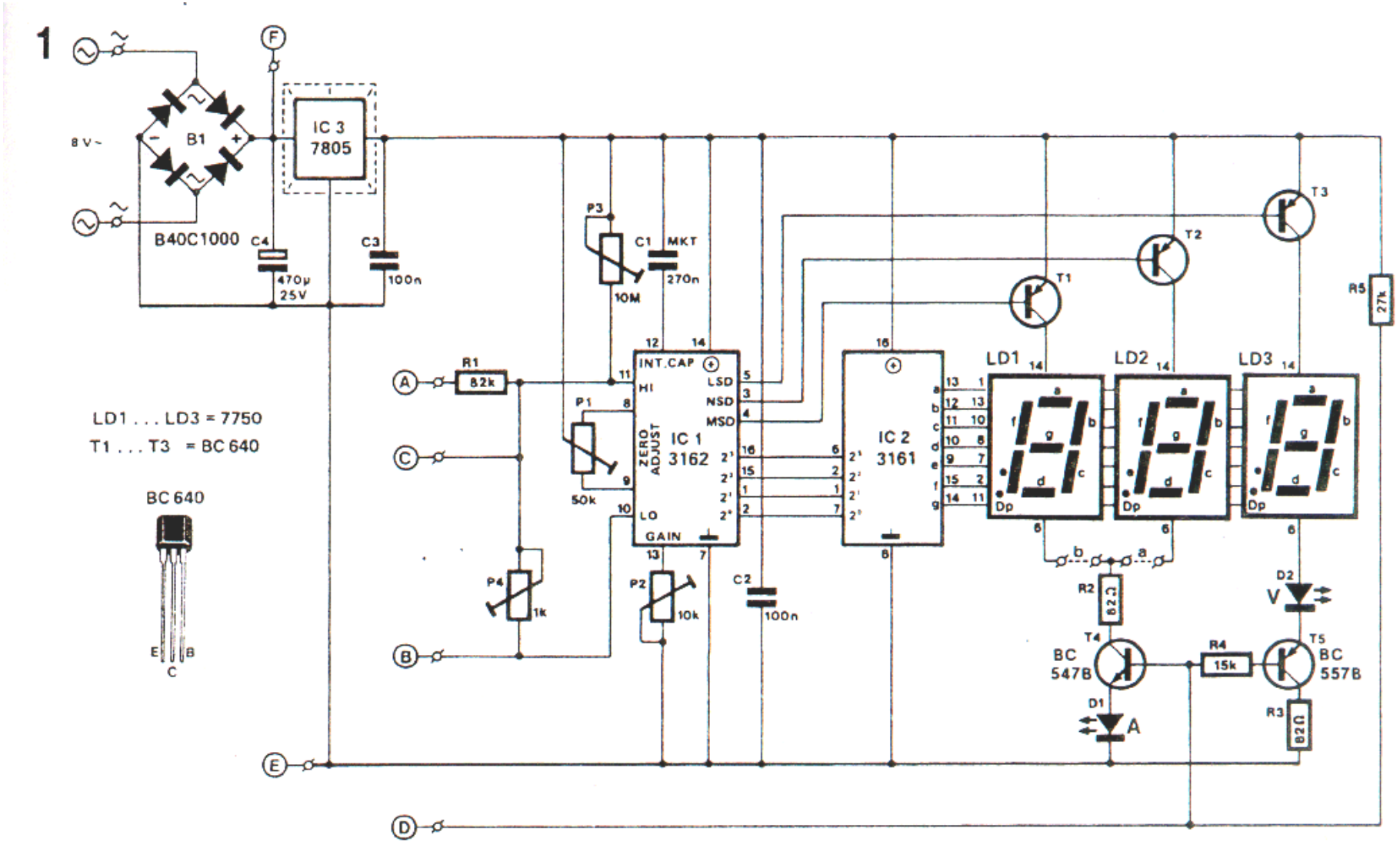
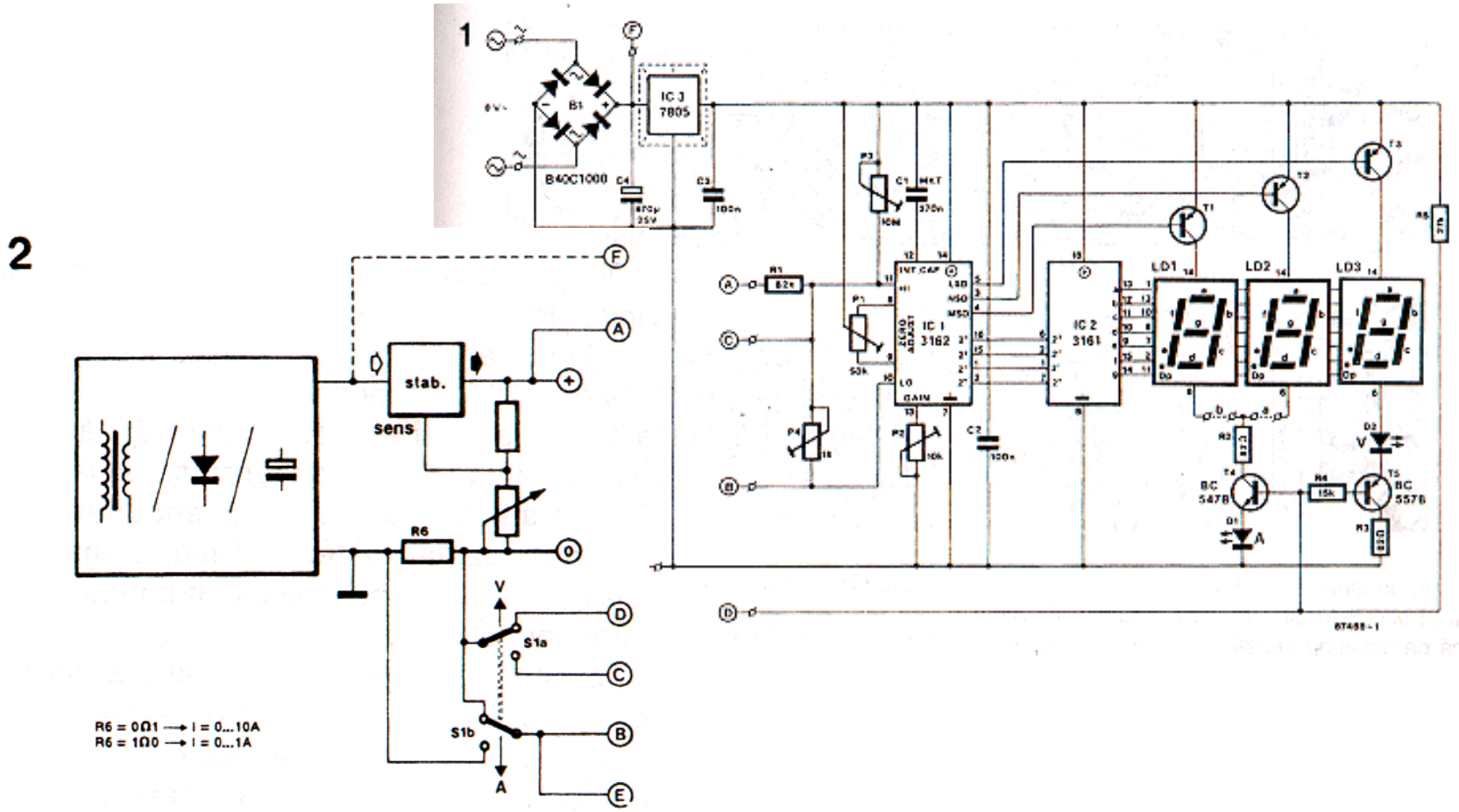
Demonstraţie în OrCAD

Modulul electronic propus ca exemplu poate fi utilizat pentru afişarea digitală a tensiunii şi curentului unei surse de alimentare de laborator existente, care nu dispune de acest afişaj.



Schema 1- Datele inițiale pentru proiectarea modulului PCB



First of all some words about the working principle of the circuit.

- **The schematics from fig. 2 will not be used, but it suggests a required intervention in the existing power supply.**
- **The main change is the insertion of the series (shunt) resistor R6.**
- **The connection of the module with the power supply will be assured by the connector pins A-F.**

Working principle (continued)

■ The switch between the U/I display mode is done by the DPDT (Double Pole Double Throw) switch S1 (not included in our PCB).

■ For voltage measurement the voltage applied to IC1 is divided by the group R1-P4 in a quotient 1:100. The decimal point of LD3 and the LED "V" are lit on, the display resolution is 0,1 V.

■ For current measurement the voltage drop at R6, is applied directly at HI-LO terminals of the DAC circuit IC1. In this case there are two possible scale connections (a) - 0÷9,99 A or connection (b)- 0÷0,999 A. In these cases the shunt resistor must have the values 0.1 Ω, respectively 1 Ω.

■ The circuit has 4 adjustment points:

•P1 null point adjustment for current domain

•P2 full scale calibration for current

•P3 null point adjustment for voltage domain

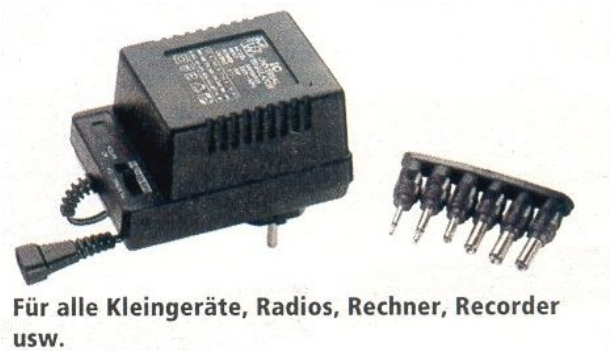
•P4 full scale calibration for voltage

The adjustments must be done in this order.

Demonstration of design flow in OrCAD

Înainte de orice activitate CAD va trebui să răspundem la câteva întrebări :

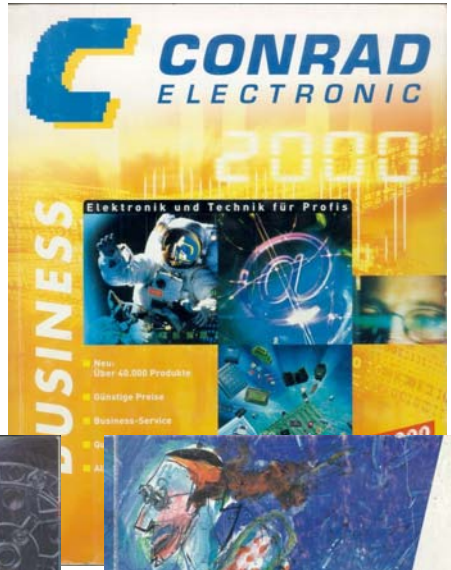
- **Cum va arăta carcasa (cutia) ?**
- **Cum este alimentat circuitul?**
- **Câte plăci -module PCB sunt necesare?**
- **Câte straturi trebuie să aibă plăcile?**
- **Câţi conectori se vor utiliza?**
- **Se vor utiliza componente SMD sau THT ? Etc.**

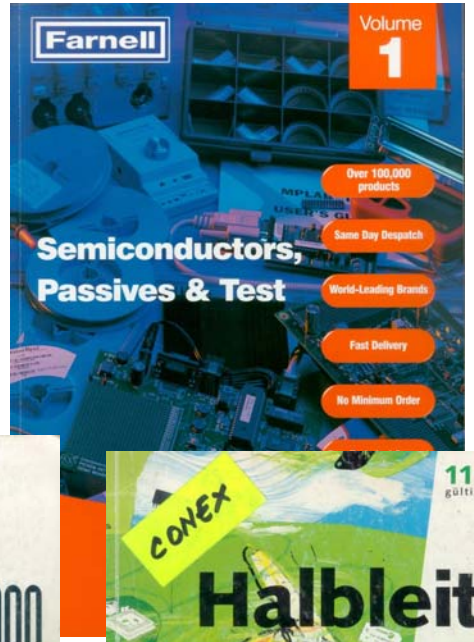


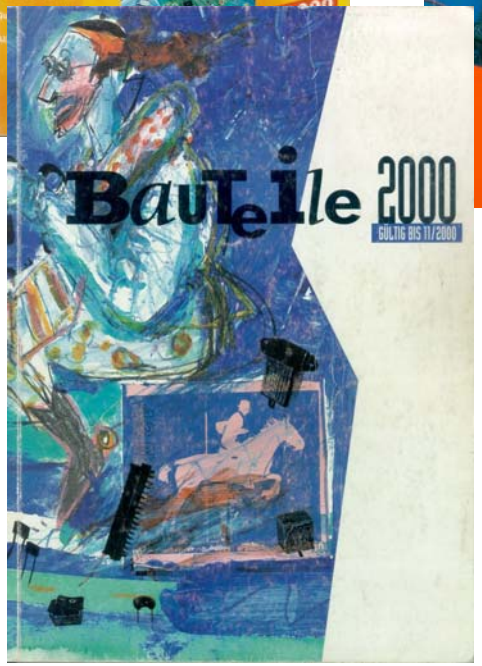
Pentru a răspunde la unele întrebări trebuie să privim proiectul CAD în ansamblu, ca parte a unui proiect de construcţie a unui aparat electronic.

PRIMA ACTIVITATE: Adunarea de informaţii despre componente

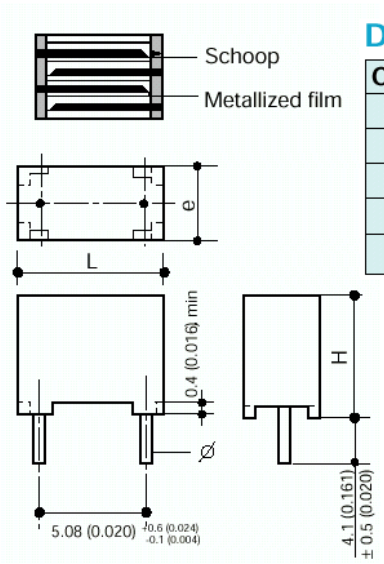
Surse: Cataloage ale distribuitorilor, foi de catalog ale fabricanţilor accesibile pe Web, etc.







Schematic Cross Section



DIMENSIONS: millimeters (inches)

Case	L max.	H max.	e max.	ø ± 0.02	Observations
01	7.5 (0.295)	6.5 (0.256)	2.5 (0.098)	0.5 (0.020)	1nF ≤ C_R ≤ 220nF
02	7.5 (0.295)	8.0 (0.315)	3.2 (0.126)	0.5 (0.020)	12nF ≤ C_R ≤ 330nF
05	7.5 (0.295)	12.0 (0.472)	6.0 (0.236)	0.5 (0.020)	560nF ≤ C_R ≤ 2.2µF
06	7.5 (0.295)	9.6 (0.378)	6.0 (0.236)	0.5 (0.020)	47nF / 400V
07	7.5 (0.295)	8.0 (0.315)	5.0 (0.197)	0.5 (0.020)	27nF ≤ C_R ≤ 1µF

C2,C3 Multilayer ceramic capacitors MCC

C5215

Keramik-Vielschicht-Kondensatoren, lose
Keramikart: NP0
Rastermaß: 5,08 mm
Hersteller: TPC, Kemet

Technische Daten

Nennspannung: 100 V DC
Kapazitätstoleranz: ± 5 %
umfassende technische Daten siehe Seite C.59

C5215 Keramik-Vielschicht-Kondensatoren NP0

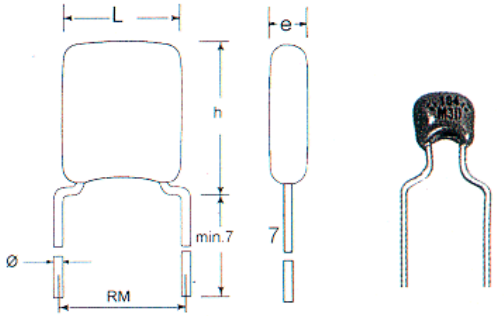
Artikel	Artikelbezeichnung
CV100PFN-5	Vs-Kond 100pF 100V NP0 RM5,08
CV150PFN-5	Vs-Kond 150pF 100V NP0 RM5,08
CV220PFN-5	Vs-Kond 220pF 100V NP0 RM5,08
CV330PFN-5	Vs-Kond 330pF 100V NP0 RM5,08
CV470PFN-5	Vs-Kond 470pF 100V NP0 RM5,08
CV680PFN-5	Vs-Kond 680pF 100V NP0 RM5,08
CV820PFN-5	Vs-Kond 820pF 100V NP0 RM5,08

C1 Metalized film capacitor

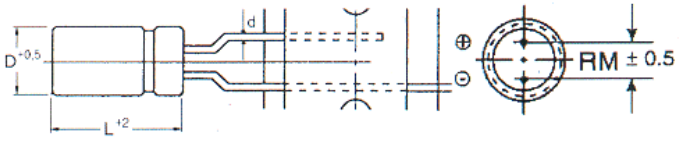
Abmessungen

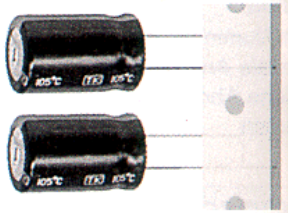
L [mm]	h [mm]	e [mm]	ø [mm]	RM [mm]
3,8	5,8	2,5	$0,5^{\pm 10\%}$	$5,08^{+0,6/-0,1}$

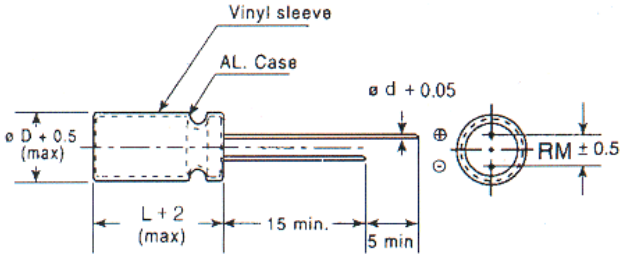
CV_PFN-5

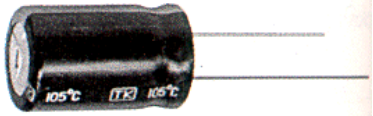


CSHT_/25









C6380

Miniatur-Elektrolyt-Kondensatoren, radiale Anschlüsse, gegurtet und lose
Temperaturbereich: -40 ... 105 °C
Nennspannung: 25 V DC

JAMICON

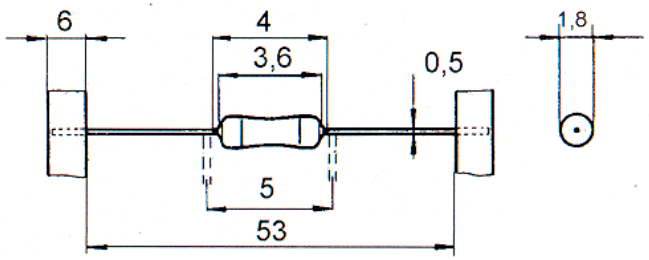
C4 Aluminium Electrolytic Capacitor

Technische Daten, Abmessungen, Lieferform

CSHT_	C	U_N	I_R	D	L	RM	d	Lieferform
	[µF]	[V=]	[mA]		[mm]			
0022/25	22	25	47	5	11	5,0	0,5	gegurtet
0100/25	100	25	110	6,3	11	5,0	0,5	gegurtet
0220/25	220	25	190	8	11	5,0	0,6	gegurtet
0470/25	470	25	340	10	16	5,0	0,6	gegurtet
1000/25	1000	25	610	13	21	5,0	0,6	lose
2200/25	2200	25	930	13	26	5,0	0,6	lose
4700/25	4700	25	1420	18	35	7,5	0,8	lose
6800/25	6800	25	1710	18	42	7,5	0,8	lose

C = Nennkapazität, U_N = Nennspannung DC, I_R = Ripple Current (85 °C, 120 Hz)

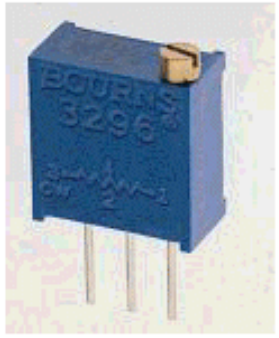
0.125W Metal Film Resistors



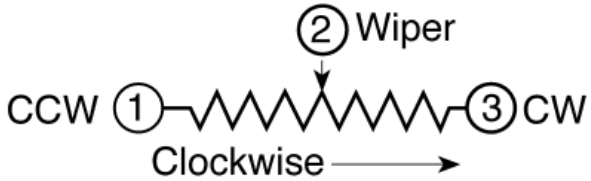
technical specification	
Rated dissipation at 70 °C	0·125 W (0·33 W commercial)
Tolerance	1%
Temperature coefficient	±50 ppm
Limiting element voltage	200V
Ambient temperature range	-55 °C to +125 °C

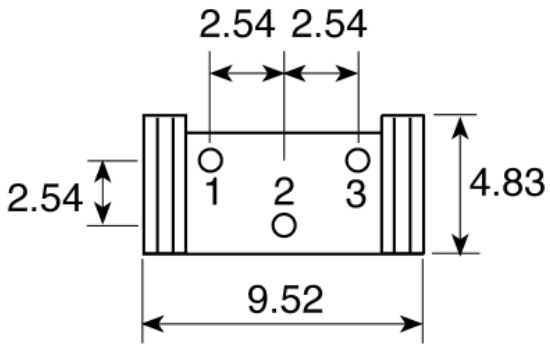
R1-R5 Metal film resistors

64Y top adjust

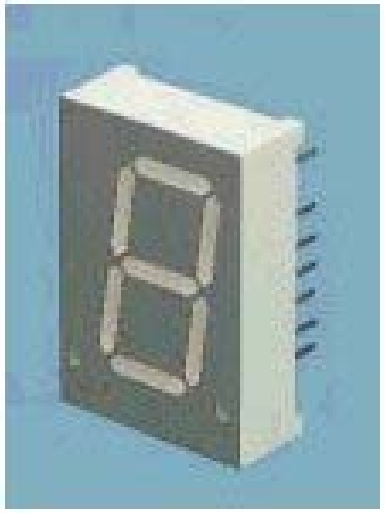


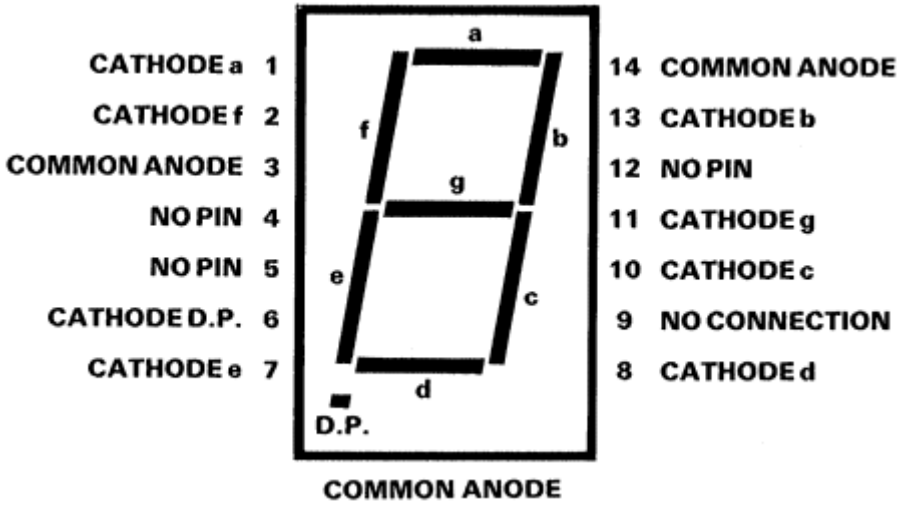
3296W top adjust





P1-P4 Multi Turn Cermet Trimmers





W. 12·7, H. 19·05, D. 6·35 (ex. pins)
Pin spacing 2·54, Row spacing 7·62

LD1-LD3 7 Segments LED Display

Short Lead Cathode
L. (Body) 8·8 Dia. 5 Lead Pitch 2·54
Leads 0·45sq.

D1-D2 LEDs for “Volts” or “Amps” Display

A3132

Brückengleichrichter 1,5 A, glaspassiviert
Gehäuse: rund

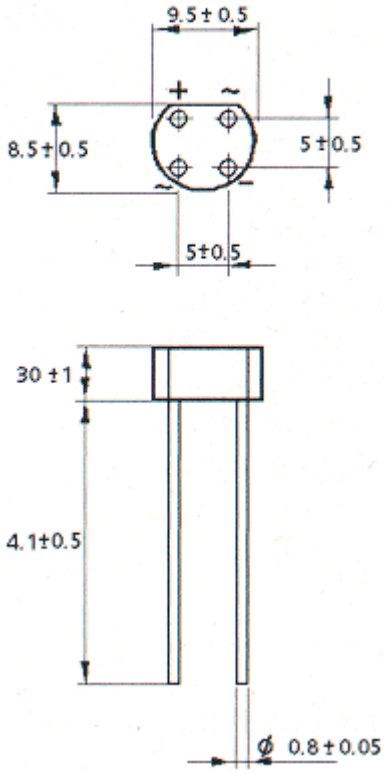
FAGOR

Technische Daten

Type	V_{RWM} [V]	V_{RMS} [V]	V_F [V]	$I_{F(AV)}$ [A]	I_R [µA]	T_j [°C]
B40C1500	100	40	1,1	1,5	10	-40 ... +150
B80C1500	200	80	1,1	1,5	10	-40 ... +150
B250C1500	600	250	1,1	1,5	10	-40 ... +150
B380C1500	900	380	1,1	1,5	10	-40 ... +150

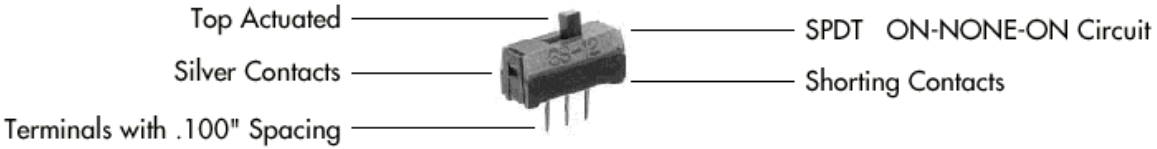
V_{RWM} = Max. peak working voltage, V_{RMS} = Recommended input voltage, V_F = Max. forward voltage drop per element at I_F = 1,5 A, $I_{F(AV)}$ = Forward current at T_{amb} = 25 °C Cload, I_R = Max. reverse current per element V_{RRM}, T_j = Operating temperature range

B_C1500

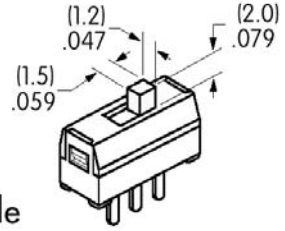


B1- 1.5 A Bridge Rectifier

SS12SDP2

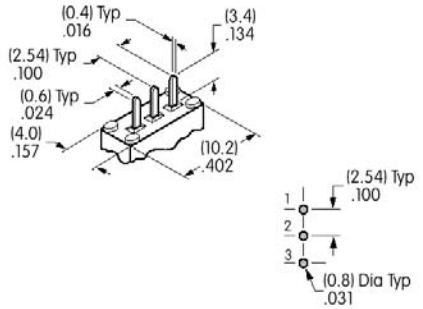


P **Top Actuated**



Through-Hole

D **Inch .100" with Gray Base**

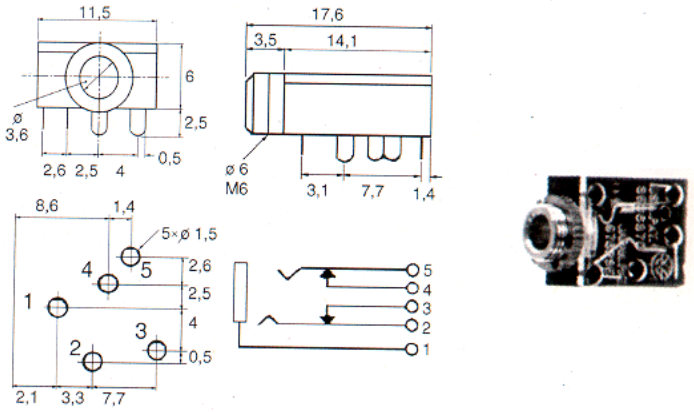


On-None-On Single Pole Models

SW1 SPDT Switch

J1 Jack female connector

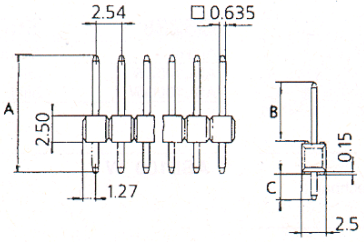
PG203JN

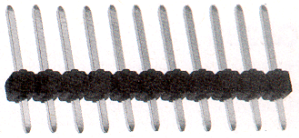


J2 In-line pins connector

G5224	Stiftleisten gerade 1-reihig RM2,54
Artikel	Artikelbezeichnung
ASL050Z	Stiftl. 50pol gerade 1R Zinn
ASL050TG	Stiftl. 50pol gerade 1R Teilgold
ASL050G	Stiftl. 50pol gerade 1R Gold

ASL050_





BC546; BC547 NPN general purpose transistors

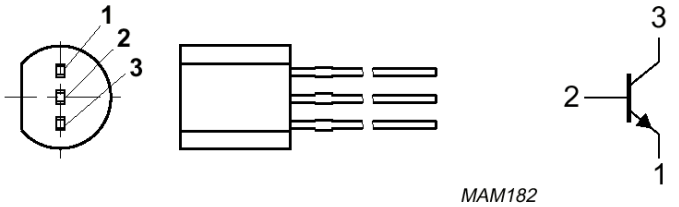


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

T4, T5 small signal transistors

BC636; BC638; BC640

PNP medium power transistors

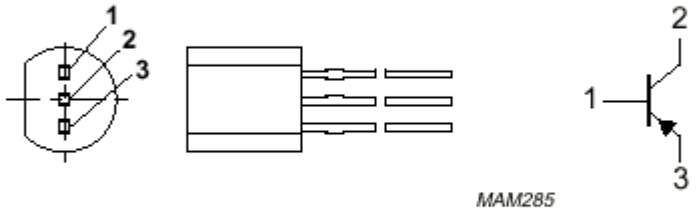


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

T1- T3 medium power transistors

HARRIS Semiconductor

CA3161

August 1997

BCD to Seven Segment Decoder/Driver

Features

- TTL Compatible Input Logic Levels
- 25mA (Typ) Constant Current Segment Outputs
- Eliminates Need for Output Current Limiting Resistors
- Pin Compatible with Other Industry Standard Decoders
- Low Standby Power Dissipation .....18mW (Typ)

Description

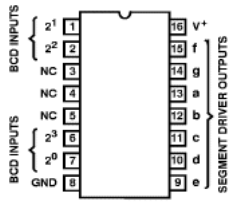
The CA3161E is a monolithic integrated circuit that performs the BCD to seven segment decoding function and features constant current segment drivers. When used with the CA3162E A/D Converter the CA3161E provides a complete digital readout system with a minimum number of external parts.

Ordering Information

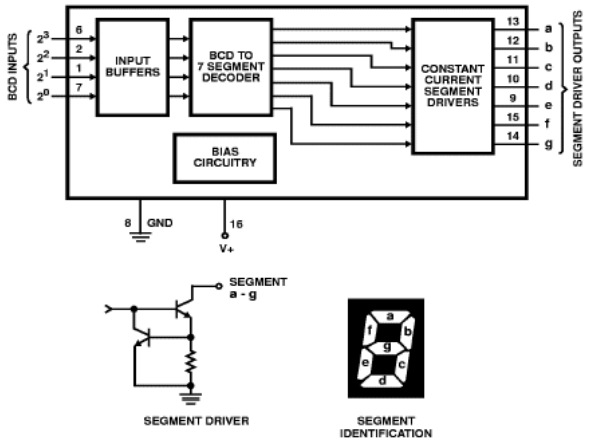
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3161E	0 to 70	16 Ld PDIP	E16.3

Pinout

CA3161
(PDIP)
TOP VIEW



Functional Block Diagram



U2 BCD Decoder

U1 A/D Converter

intersil

CA3162

April 2002

A/D Converters for 3-Digit Display

Features

- Dual Slope A/D Conversion
- Multiplexed BCD Display
- Ultra Stable Internal Band Gap Voltage Reference
- Capable of Reading 99mV Below Ground with Single Supply
- Differential Input
- Internal Timing - No External Clock Required
- Choice of Low Speed (4Hz) or High Speed (96Hz) Conversion Rate
- "Hold" Inhibits Conversion but Maintains Delay
- Overrange Indication
  - "EEE" for Reading Greater than +999mV, "-" for Reading More Negative than -99mV When Used With CA3161E

Description

The CA3162E and CA3162AE are I^2L monolithic A/D converters that provide a 3 digit multiplexed BCD output. They are used with the CA3161E BCD-to-Seven-Segment Decoder/Driver and a minimum of external parts to implement a complete 3-digit display. The CA3162AE is identical to the CA3162E except for an extended operating temperature range.

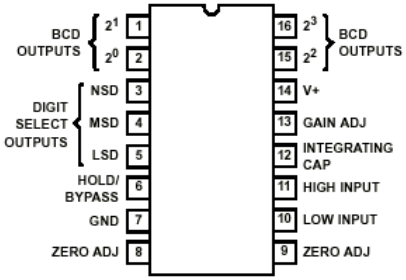
The CA3161E is described in the Display Drivers section of this data book.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3162E	0 to 70	16 Ld PDIP	E16.3

Pinout

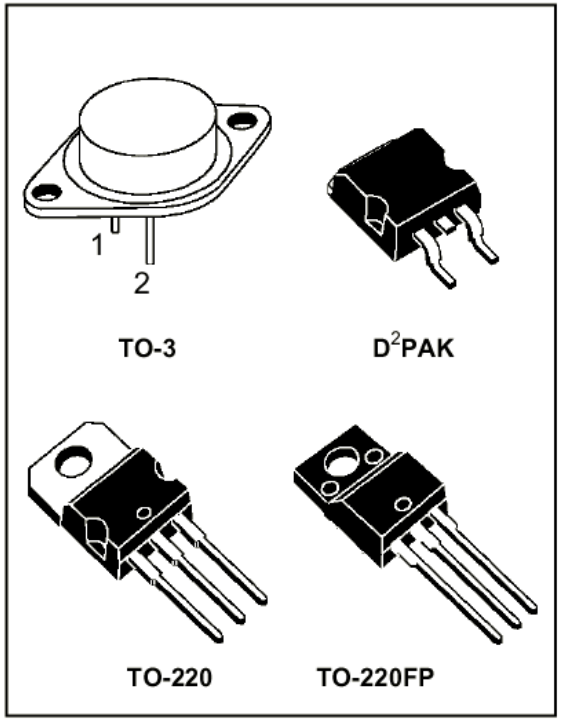
CA3162 (PDIP)
TOP VIEW



L7800 SERIES

POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5 A
- OUTPUT VOLTAGES OF 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSITION SOA PROTECTION

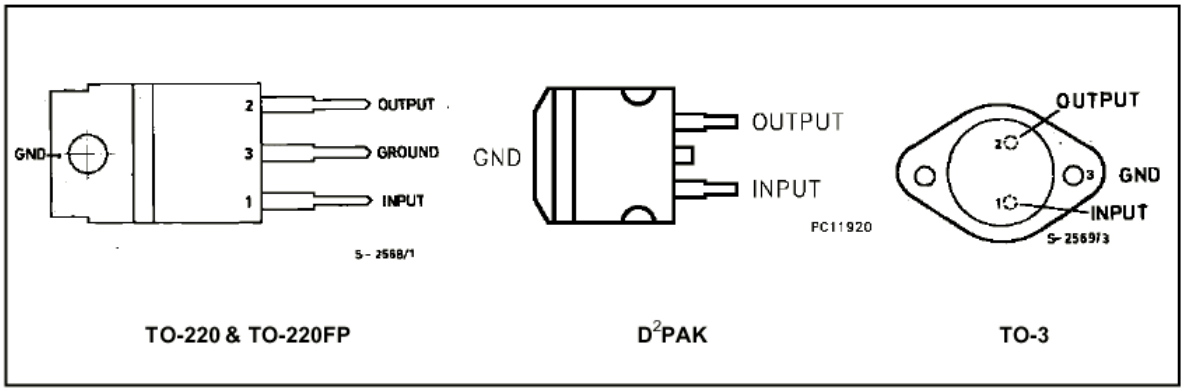


DESCRIPTION

The L7800 series of three-terminal positive regulators is available in TO-220 TO-220FP TO-3 and D^2PAK packages and several fixed output voltages, making it useful in a wide range of applications.These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

U3 Voltage Regulator

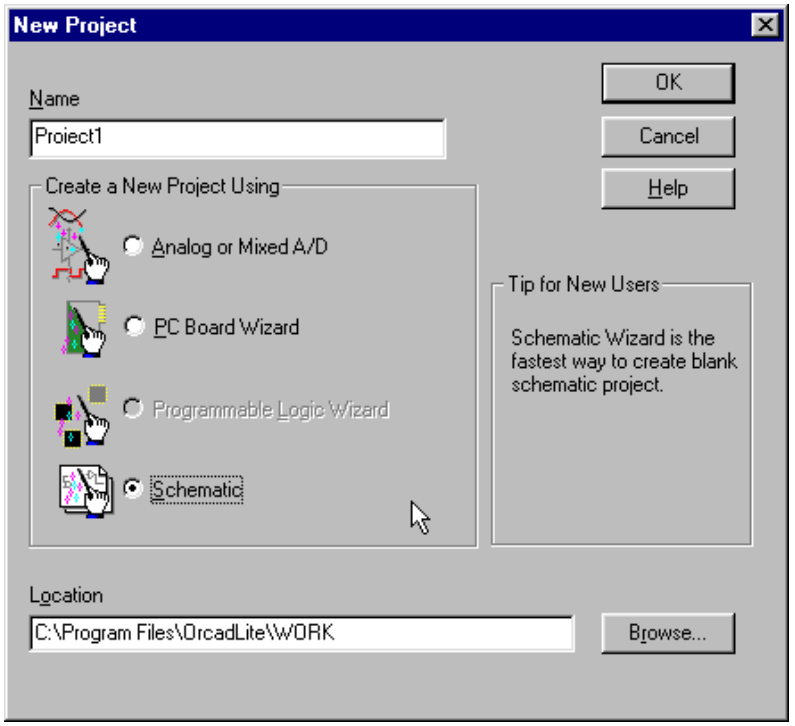
CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

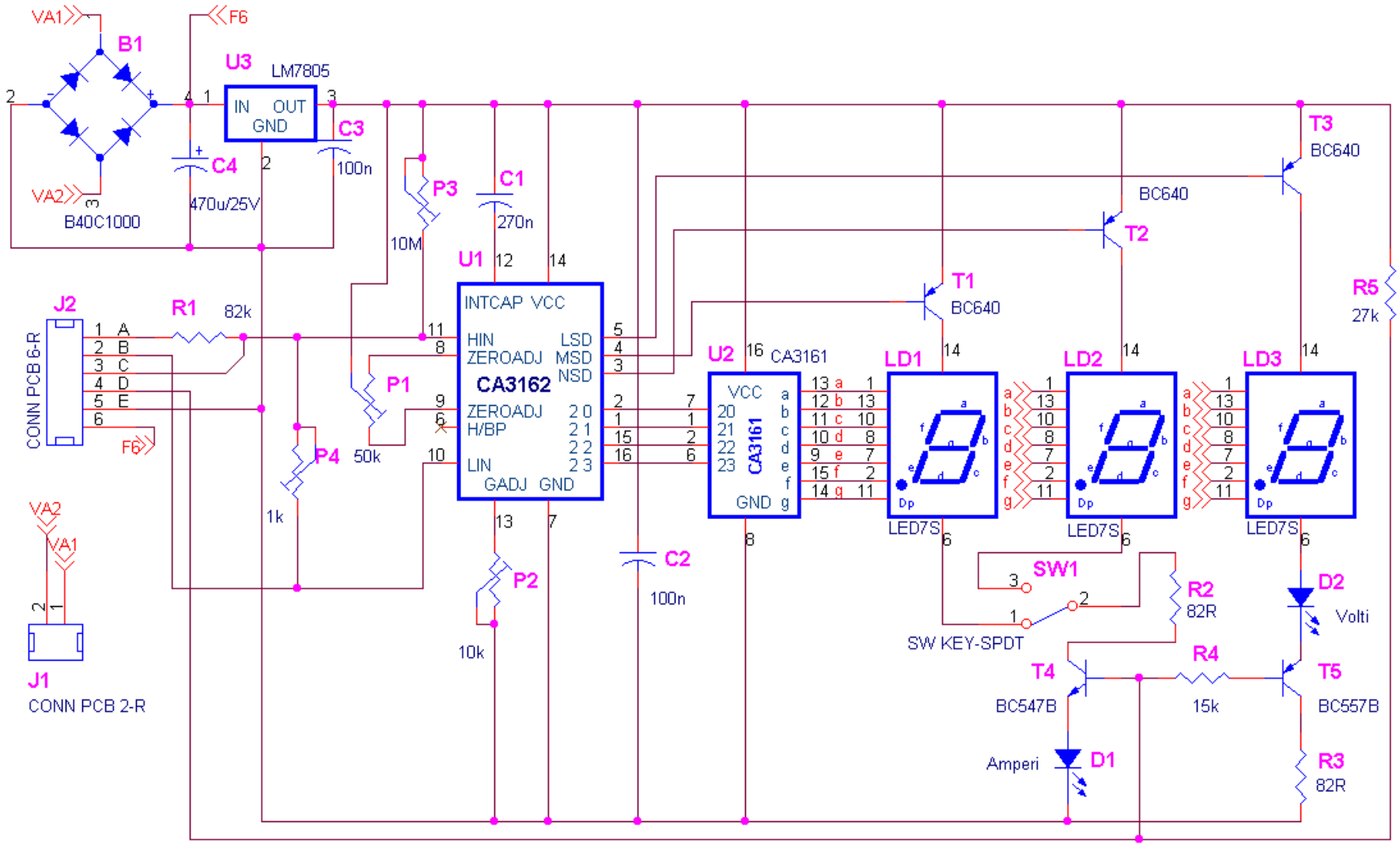


NEXT STEP:

Realization of the Schematic Drawing

File → New Project

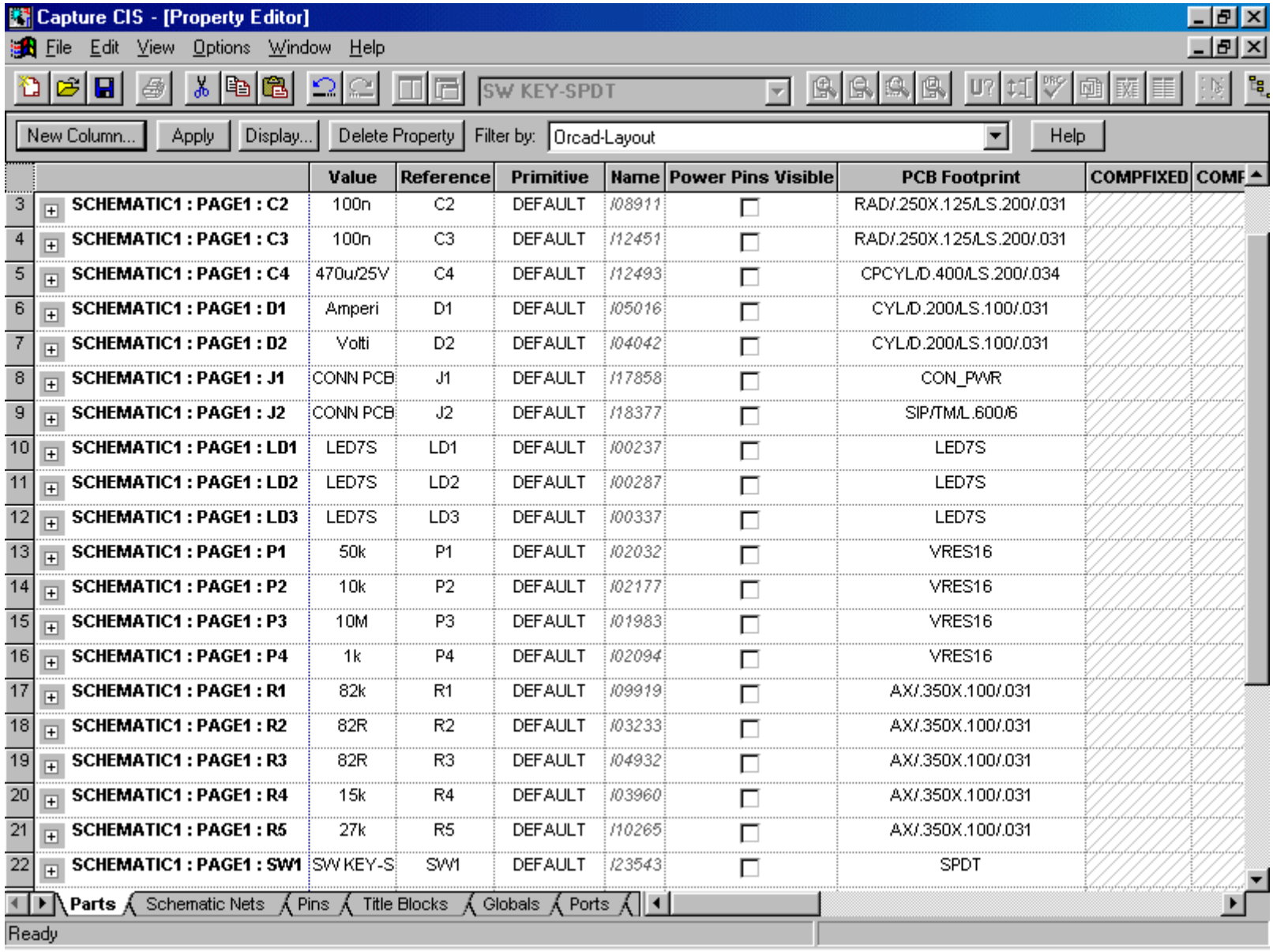




Schematic Page of the module as apears in Capture

Art.	Qty.	Ref.	Value	Part Name/Library	PCB Footprint (Library)
1	1	B1	B40C1000	BRIDGE/DISCRETE	BR_40– **new created**
2	1	C1	270n	CAP/DISCRETE	RAD/.300X.125/LS.200/.031 (TM_RAD)
3	2	C2,C3	100n	CAP/DISCRETE	RAD/.250X.125/LS.200/.031 (TM_RAD)
4	1	C4	470u/25V	CAP POL/DISCRETE	CPCYL/D.400/LS.200/.034 (TM_CAP_P)
5	1	D1	Ampers	LED/DISCRETE	CYL/D.200/LS.100/.031 (TM_CYLND)
6	1	D2	Volts	LED/DISCRETE	CYL/D.200/LS.100/.031 (TM_CYLND)
7	1	J1	CONN PCB 2-R	CONN PCB 2-R/CONNECTOR	CON_PWR- **new created**
8	1	J2	CONN PCB 6-R	CONN PCB 6-R/ CONNECTOR	SIP/TM/L.600/6 (SIP)
9	3	LD1,2,3	LED7S	LED7S-**new created**	LED7S- **new created**
10	1	P1	50k	TRIM– **new created**	VRES16 (VRES)
11	1	P2	10k	TRIM – **new created**	VRES16 (VRES)
12	1	P3	10M	TRIM – **new created**	VRES16 (VRES)
13	1	P4	1k	TRIM – **new created**	VRES16 (VRES)
14	1	R1	82k	R/DISCRETE	AX/.350X.100/.031 (TM_AXIAL)
15	2	R2	82R	R/DISCRETE	AX/.350X.100/.031 (TM_AXIAL)
		R3	82R	R/DISCRETE	AX/.350X.100/.031 (TM_AXIAL)
16	1	R4	15k	R/DISCRETE	AX/.350X.100/.031 (TM_AXIAL)
17	1	R5	27k	R/DISCRETE	AX/.350X.100/.031 (TM_AXIAL)
18	1	SW1	SW KEY-SPDT	SW KEY-SPDT/DISCRETE	SPDT- **new created**
19	3	T1,T2,T3	BC640	BC640/TRANSISTOR	TO92/100 (TO)
20	1	T4	BC547B	BC547B/TRANSISTOR	TO92/100 (TO)
21	1	T5	BC557B	BC557/TRANSISTOR	TO92/100 (TO)
22	1	U1	CA3162	CA3162- **new created**	DIP.100/16/W.300/L.800 (DIP100T)
23	1	U2	CA3161	CA3161- **new created**	DIP.100/16/W.300/L.800 (DIP100T)
24	1	U3	LM7805	LM7805- **new created**	TO220AB (TO)

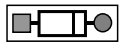
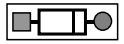
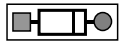
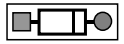
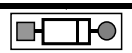
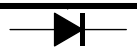
Some parts (symbols) or/and footprints must be created



		Value	Reference	Primitive	Name	Power Pins Visible	PCB Footprint	COMPFIXED	COMF
3	SCHEMATIC1 : PAGE1 : C2	100n	C2	DEFAULT	/08911		RAD/.250X.125/LS.200/.031		
4	SCHEMATIC1 : PAGE1 : C3	100n	C3	DEFAULT	/12451		RAD/.250X.125/LS.200/.031		
5	SCHEMATIC1 : PAGE1 : C4	470u/25V	C4	DEFAULT	/12493		CPCYL/D.400/LS.200/.034		
6	SCHEMATIC1 : PAGE1 : D1	Amperi	D1	DEFAULT	/05016		CYL/D.200/LS.100/.031		
7	SCHEMATIC1 : PAGE1 : D2	Volti	D2	DEFAULT	/04042		CYL/D.200/LS.100/.031		
8	SCHEMATIC1 : PAGE1 : J1	CONN PCB	J1	DEFAULT	/17858		CON_PWR		
9	SCHEMATIC1 : PAGE1 : J2	CONN PCB	J2	DEFAULT	/18377		SIP/TM/L.600/6		
10	SCHEMATIC1 : PAGE1 : LD1	LED7S	LD1	DEFAULT	/00237		LED7S		
11	SCHEMATIC1 : PAGE1 : LD2	LED7S	LD2	DEFAULT	/00287		LED7S		
12	SCHEMATIC1 : PAGE1 : LD3	LED7S	LD3	DEFAULT	/00337		LED7S		
13	SCHEMATIC1 : PAGE1 : P1	50k	P1	DEFAULT	/02032		VRES16		
14	SCHEMATIC1 : PAGE1 : P2	10k	P2	DEFAULT	/02177		VRES16		
15	SCHEMATIC1 : PAGE1 : P3	10M	P3	DEFAULT	/01983		VRES16		
16	SCHEMATIC1 : PAGE1 : P4	1k	P4	DEFAULT	/02094		VRES16		
17	SCHEMATIC1 : PAGE1 : R1	82k	R1	DEFAULT	/09919		AX/.350X.100/.031		
18	SCHEMATIC1 : PAGE1 : R2	82R	R2	DEFAULT	/03233		AX/.350X.100/.031		
19	SCHEMATIC1 : PAGE1 : R3	82R	R3	DEFAULT	/04932		AX/.350X.100/.031		
20	SCHEMATIC1 : PAGE1 : R4	15k	R4	DEFAULT	/03960		AX/.350X.100/.031		
21	SCHEMATIC1 : PAGE1 : R5	27k	R5	DEFAULT	/10265		AX/.350X.100/.031		
22	SCHEMATIC1 : PAGE1 : SW1	SW KEY-S	SW1	DEFAULT	/23543		SPDT		

Preparing Capture for transfer - Properties Editor

The correspondence symbol-footprint (SCM-PCB) at Netlist transfer in Orcad.

	Schematic Capture	PCB Layout	Obs.
1	 Pin name 1 2 Pin number — —	 Pin name 1 2	Correspondence realized correctly.
2	 Pin name A K Pin number — —	 Pin name A K	Correspondence realized correctly.
3	 Pin name A K Pin number 1 2	 Pin name 1 2	Correspondence realized correctly.
4	 Pin name A K Pin number — —	 Pin name 1 2	No correspondence found. Error at AutoECO run.
5	 Pin name 1 2 Pin number 2 1	 Pin name 1 2	Attention! The correspondence is found, but with wrong results. The field “Pin number” has priority.
6	 Pin name 1 2 Pin number * *	 Pin name 1 2	No correspondence found. Error at AutoECO run. * = any character different from those found in field “Pin name” from Layout. (1 resp. 2)

Recommendation:

- Use numbers, majority of Layout libraries use numbers.

Exceptions: TM_CAP_P, TM_DIODE.

- Modify symbols (parts) in libraries not in Schematic Page.
- Take your time and think twice!

TRANSFER TO LAYOUT

- The field “PCB Footprint” must be filled in (correctly).
- DRC Verification.
- Postprocessing: Netlist, Bill of Materials, Printing.
- Nets verification - Not a CAD activity!!!

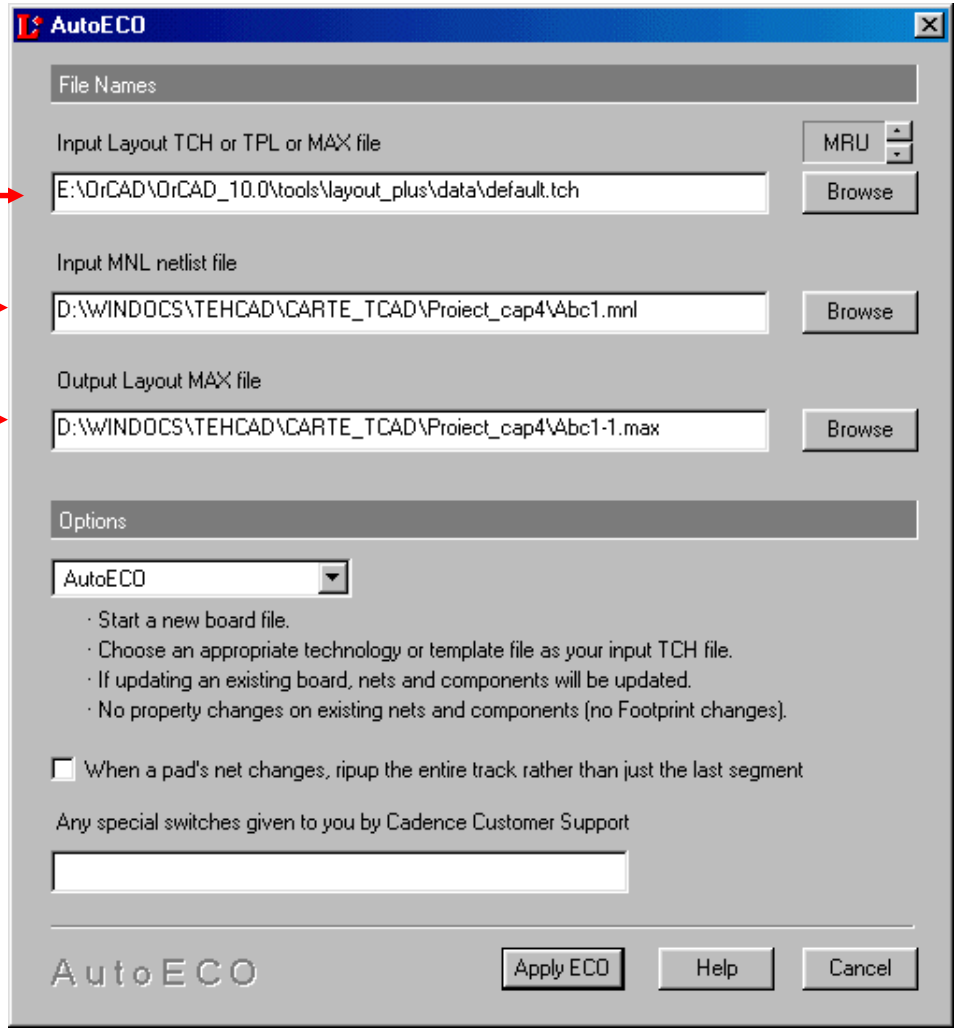
Import of Netlist in Layout Block:

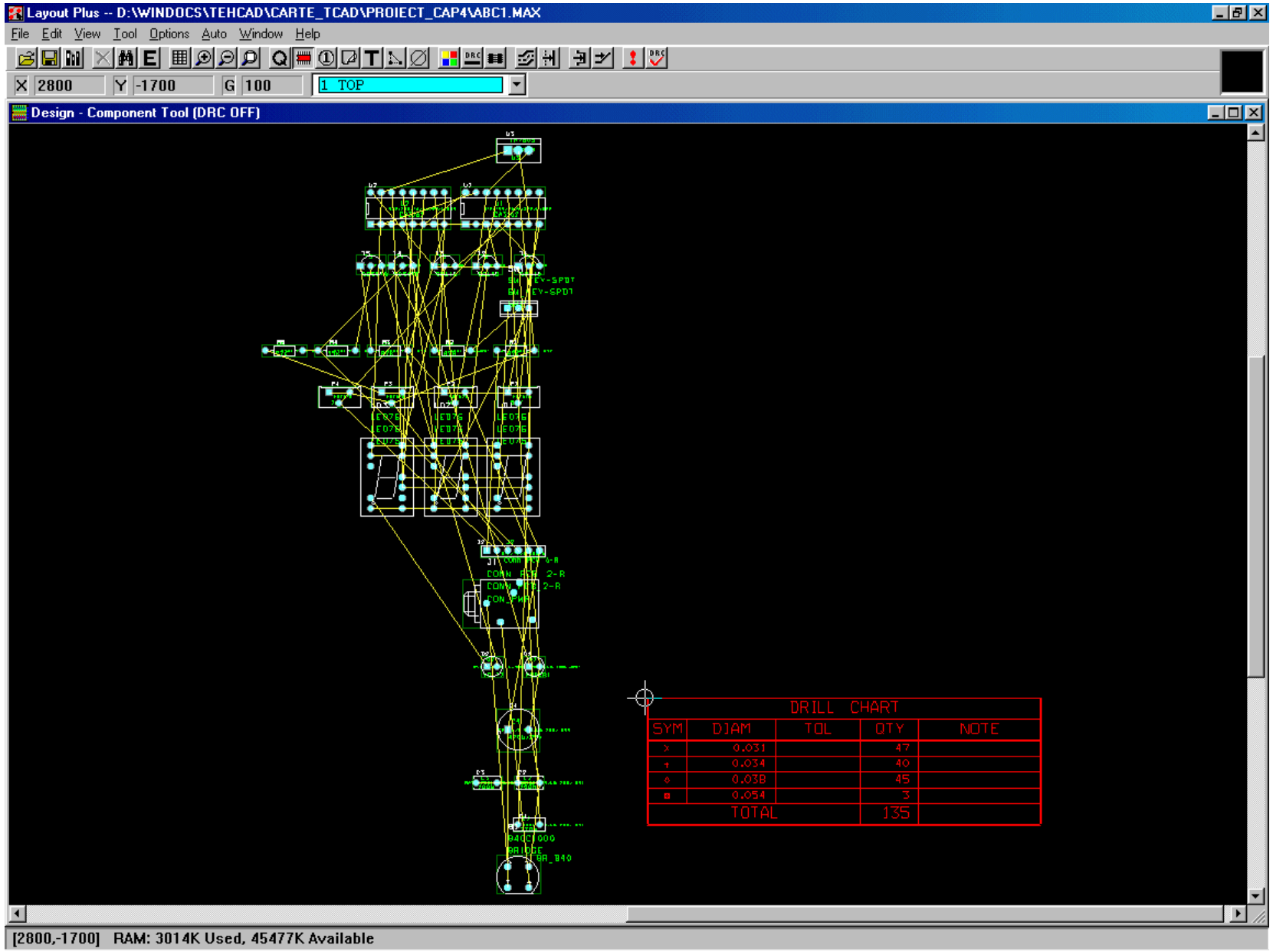
File → New

Technology template

Netlist

Layout file





Layout screen after import of the Netlist

In LAYOUT Block:

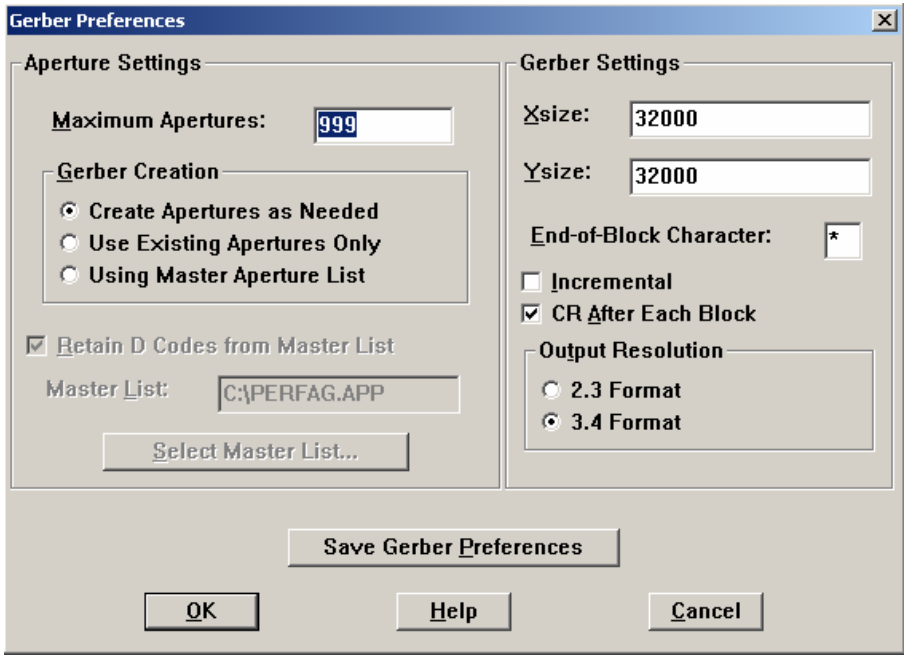
Establishment of design restrictions:

- **board outline**
- **no. of layers**
- **track widths**
- **padstack assignments**
- **route spacing**

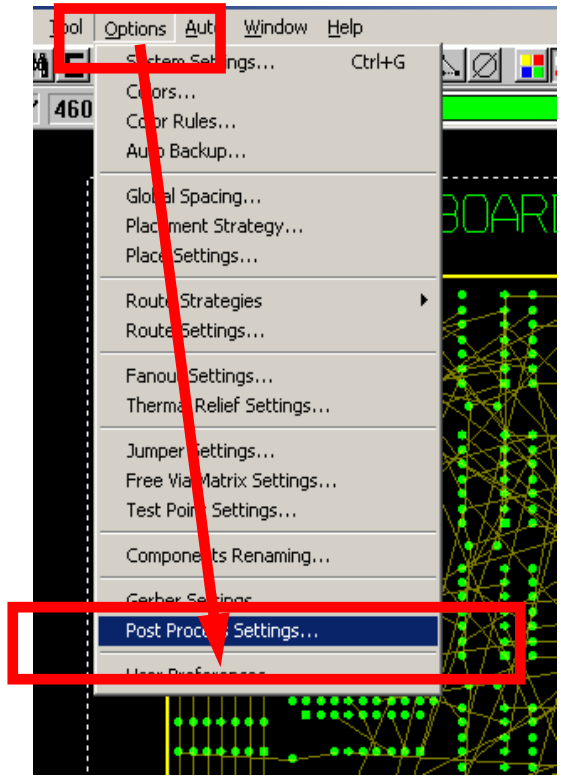
- **Component placement**
- **Routing**
- **DRC and final operations**
- **Postprocessing: Gerber and NC Drill files, Printing, Reports**

POST-PROCESSING

Options→ Gerber Settings

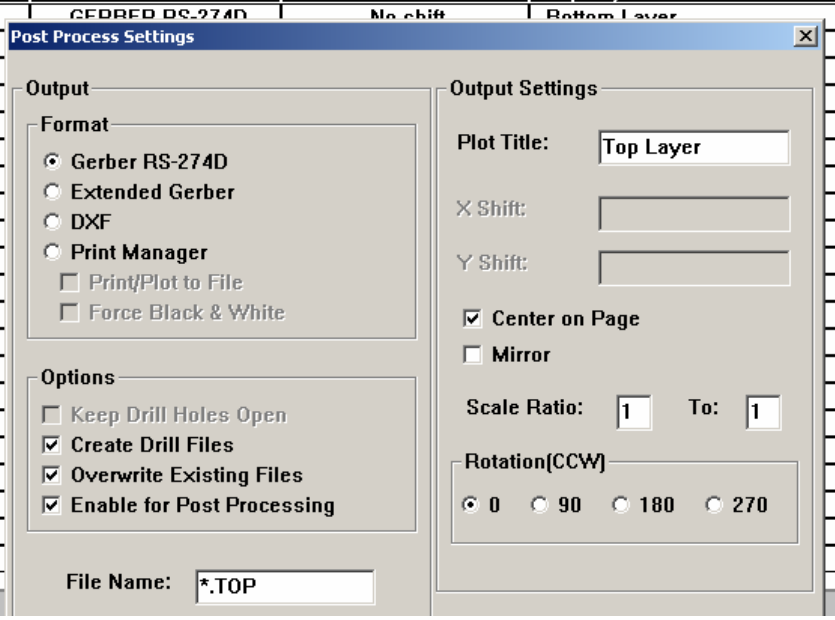


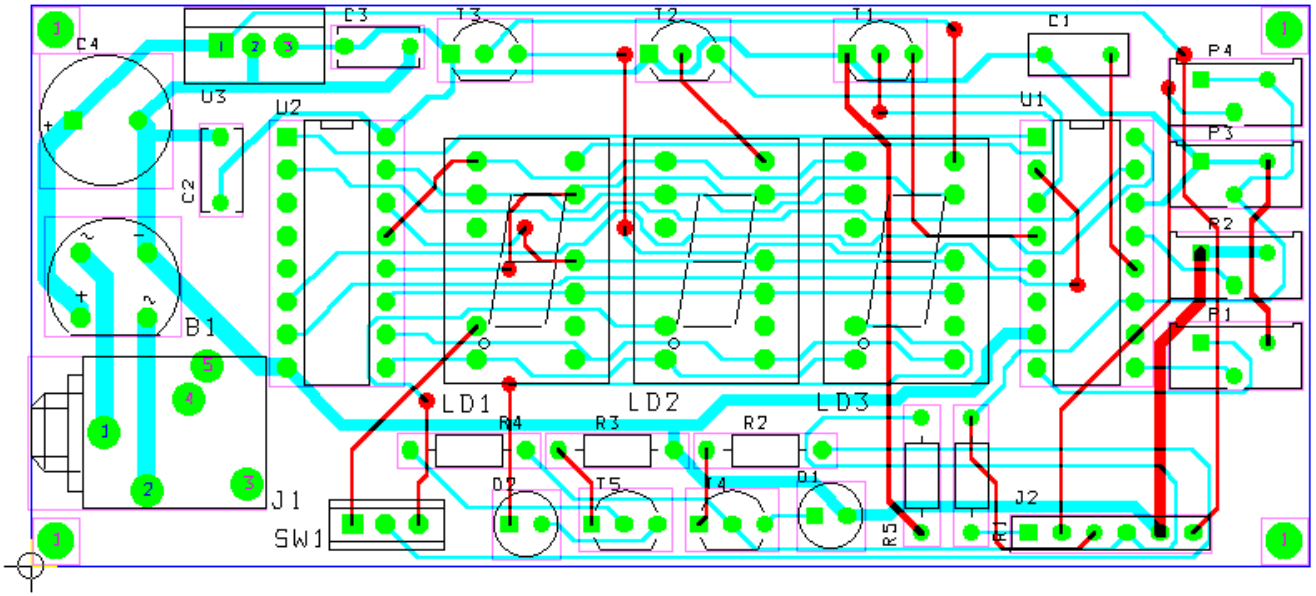
Options→ Post Process Settings



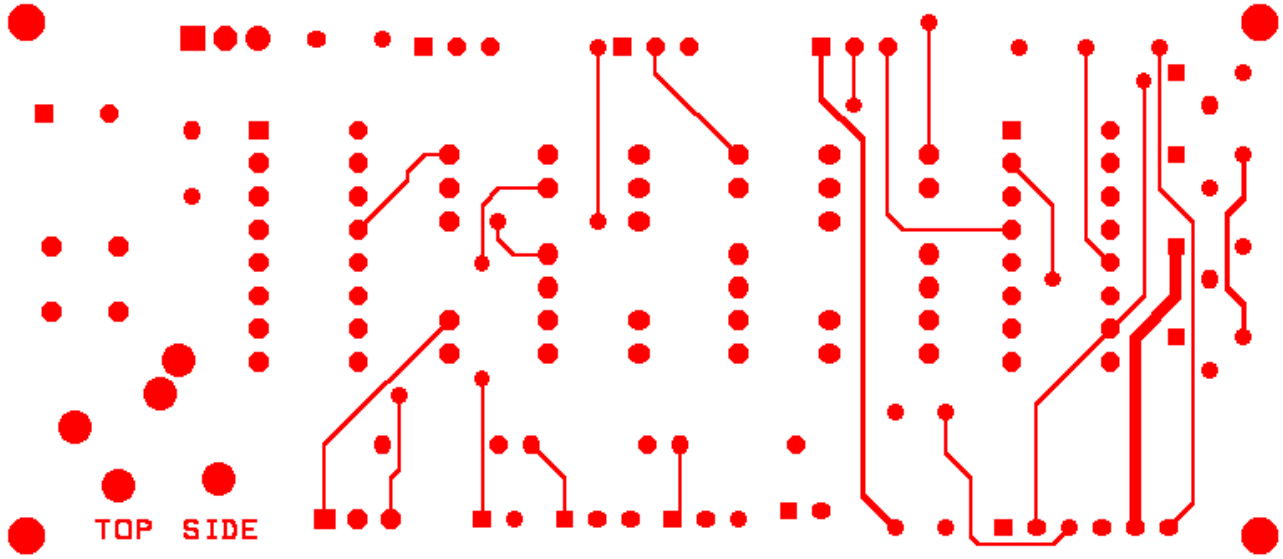
Plot output File Name	Batch Enabled	Device	Shift	Plot Title
*.TOP	Yes	GERBER RS-274D	No shift	Top Layer
*.BOT	Yes			
*.GND	Yes			
*.PWR	Yes			
*.IN1	No			
*.IN2	No			
*.IN3	No			
*.IN4	No			
*.IN5	No			
*.IN6	No			
*.IN7	No			
*.IN8	No			
*.IN9	No			
*.I10	No			
*.I11	No			
*.I12	No			
*.SMT	Yes			
*.SMB	Yes			
*.SPT	No			
*.SPB	No			
*.SST	Yes			
*.SSB	No			

Select OK to Modify or Cancel to

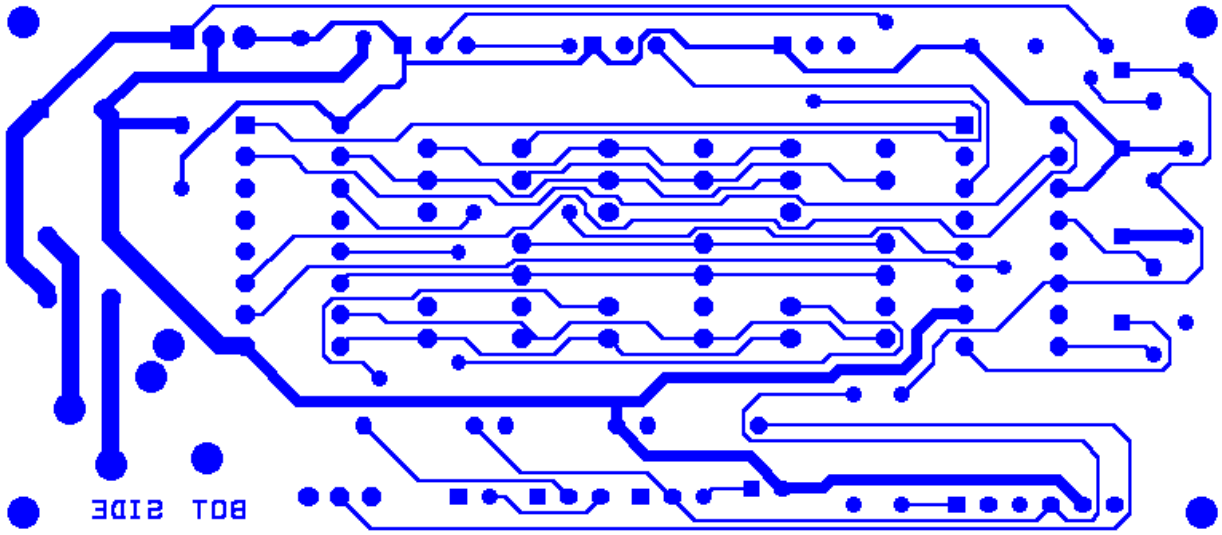




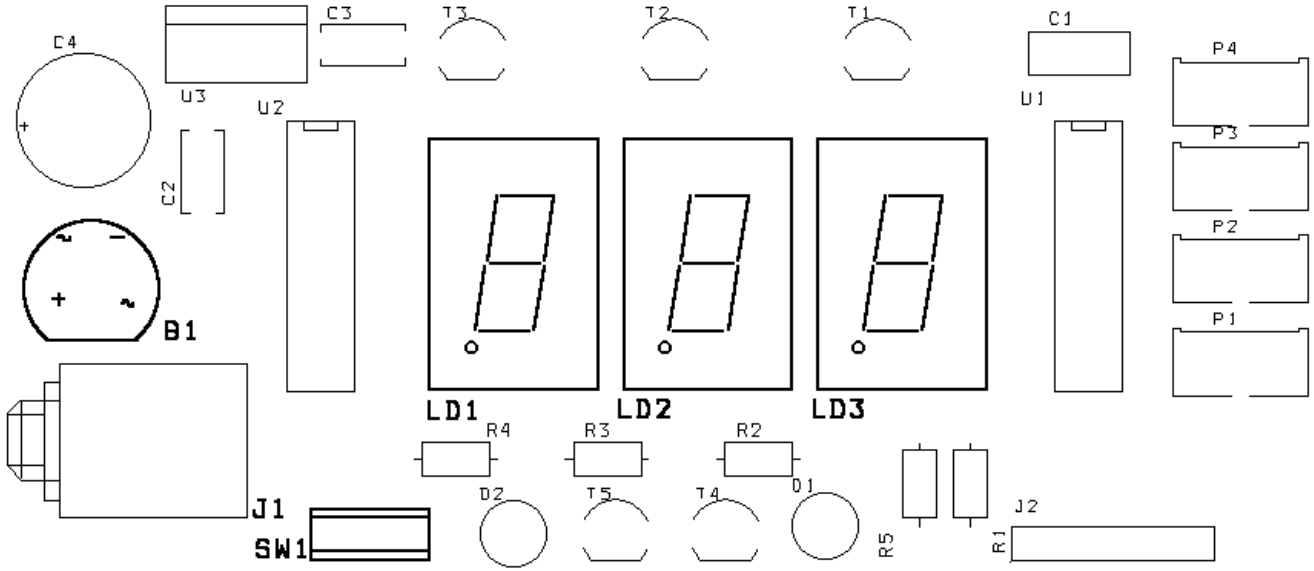
Proiect finalizat în Orcad Layout



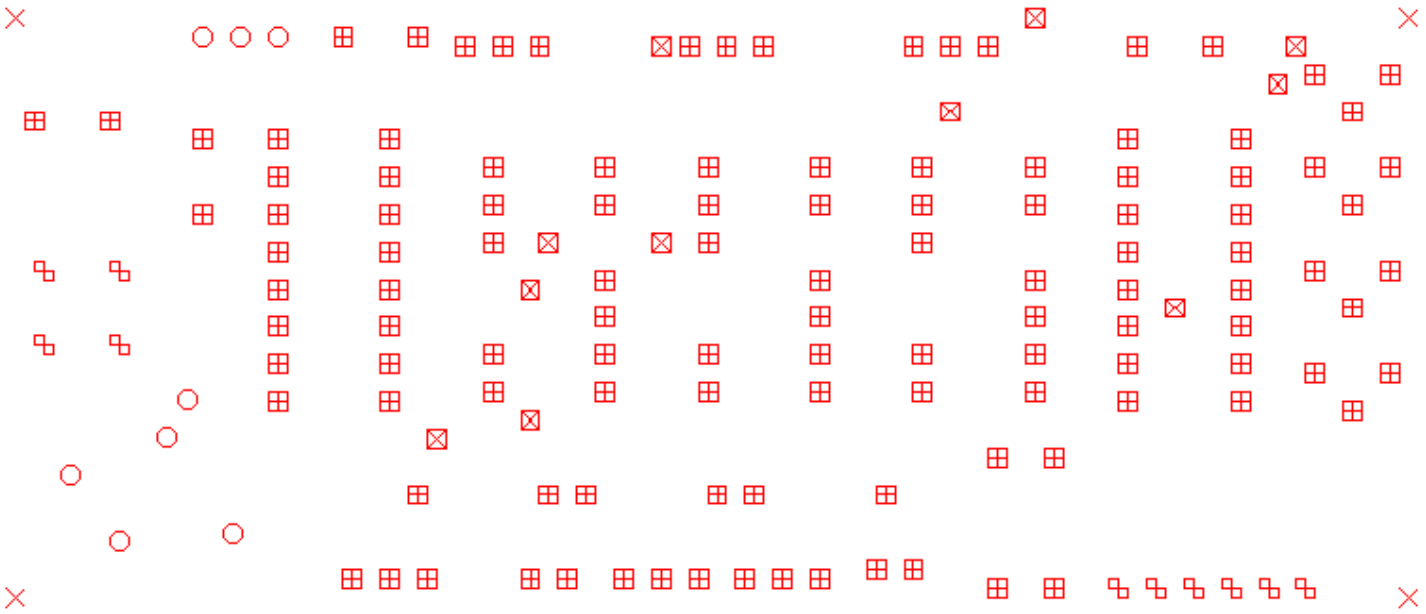
Postprocesare Top layer



Postprocesare- Bottom layer

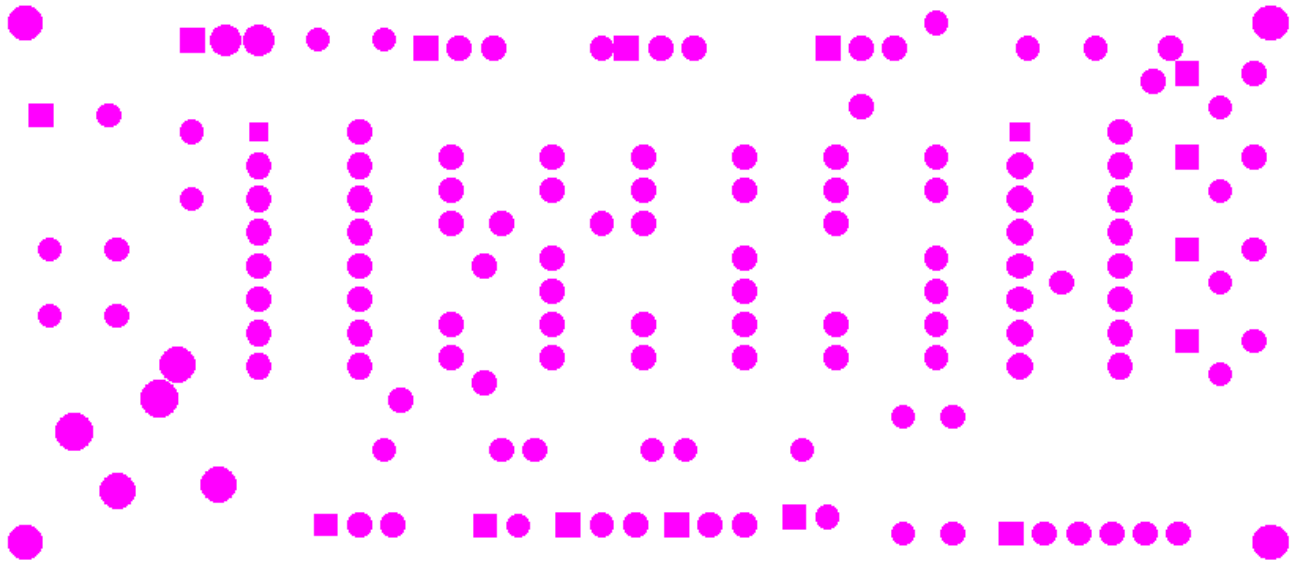


Postprocesare Masca de inscripţionare -Silk Mask

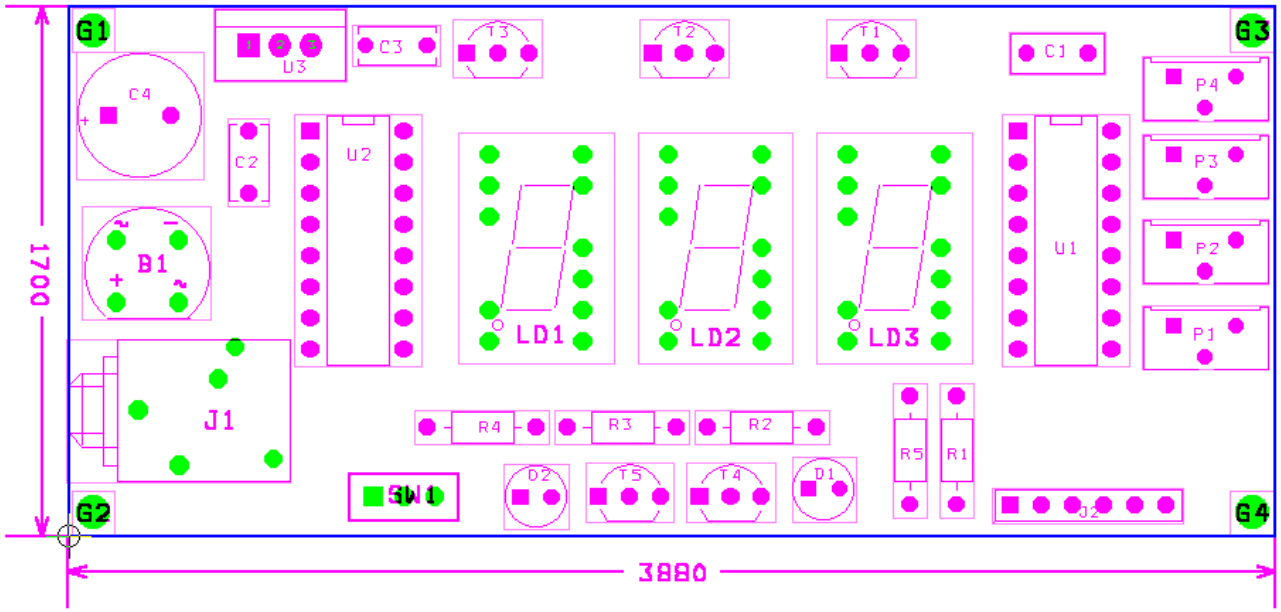


DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
⊠	0.028		11	
⊞	0.032		117	
⧉	0.036		10	
○	0.060		8	
×	0.120		4	
TOTAL			150	

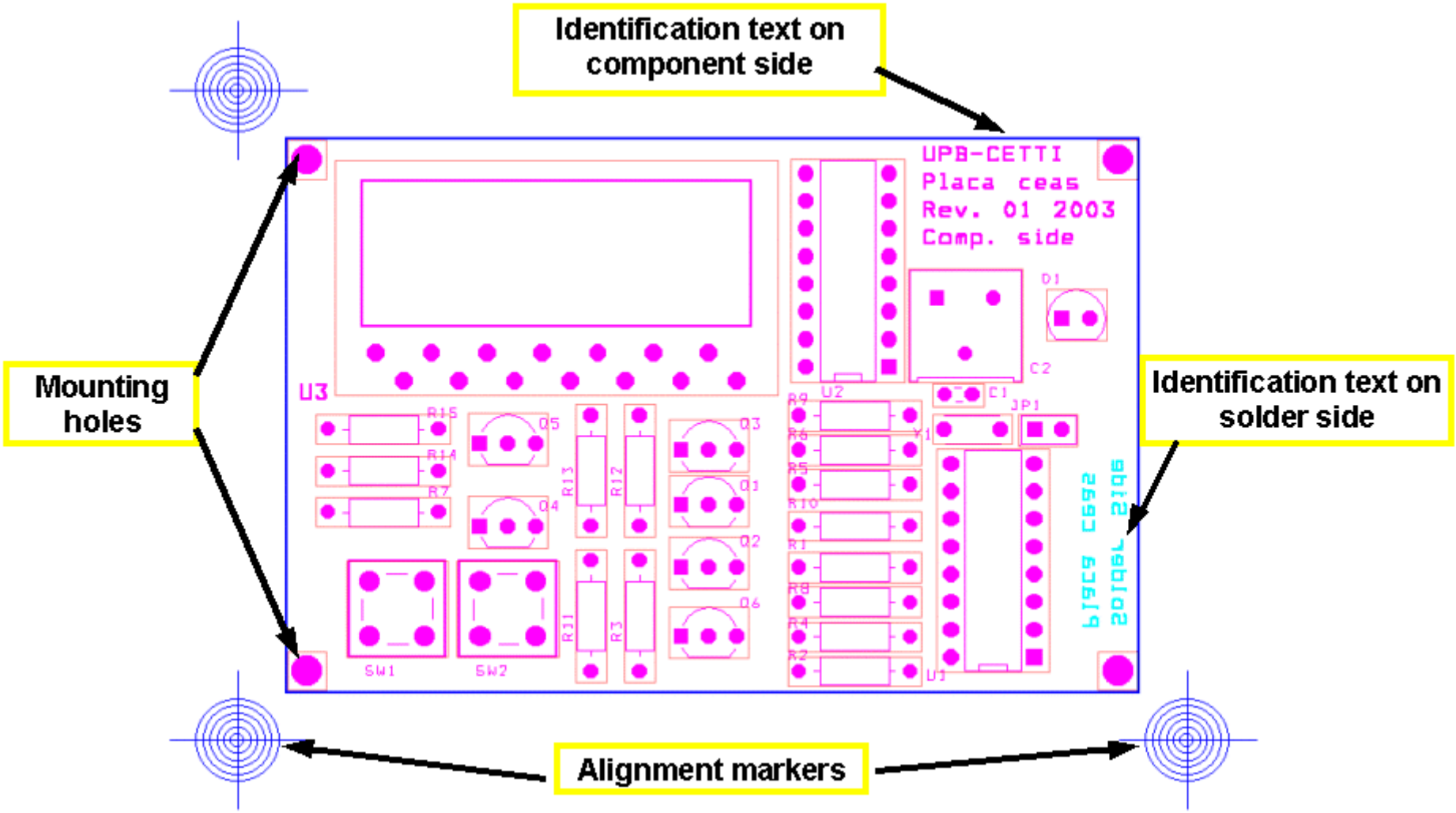
Postprocesare Drill Drawing



Postprocesare Solder Mask



Postprocesare- Assembly Drawing



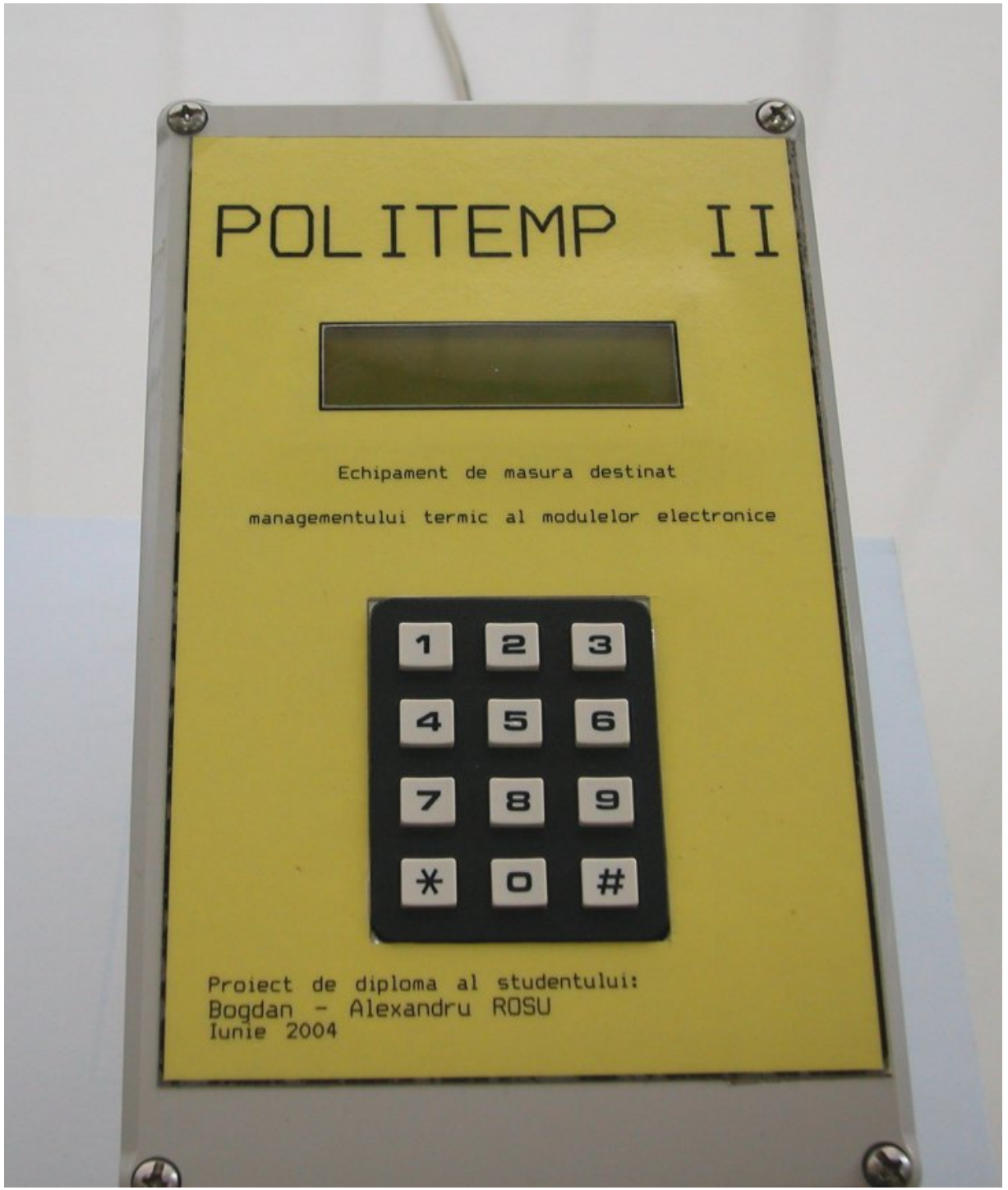
Exemple de operaţii finale

Presentation of the thermal data acquisition system Politemp II

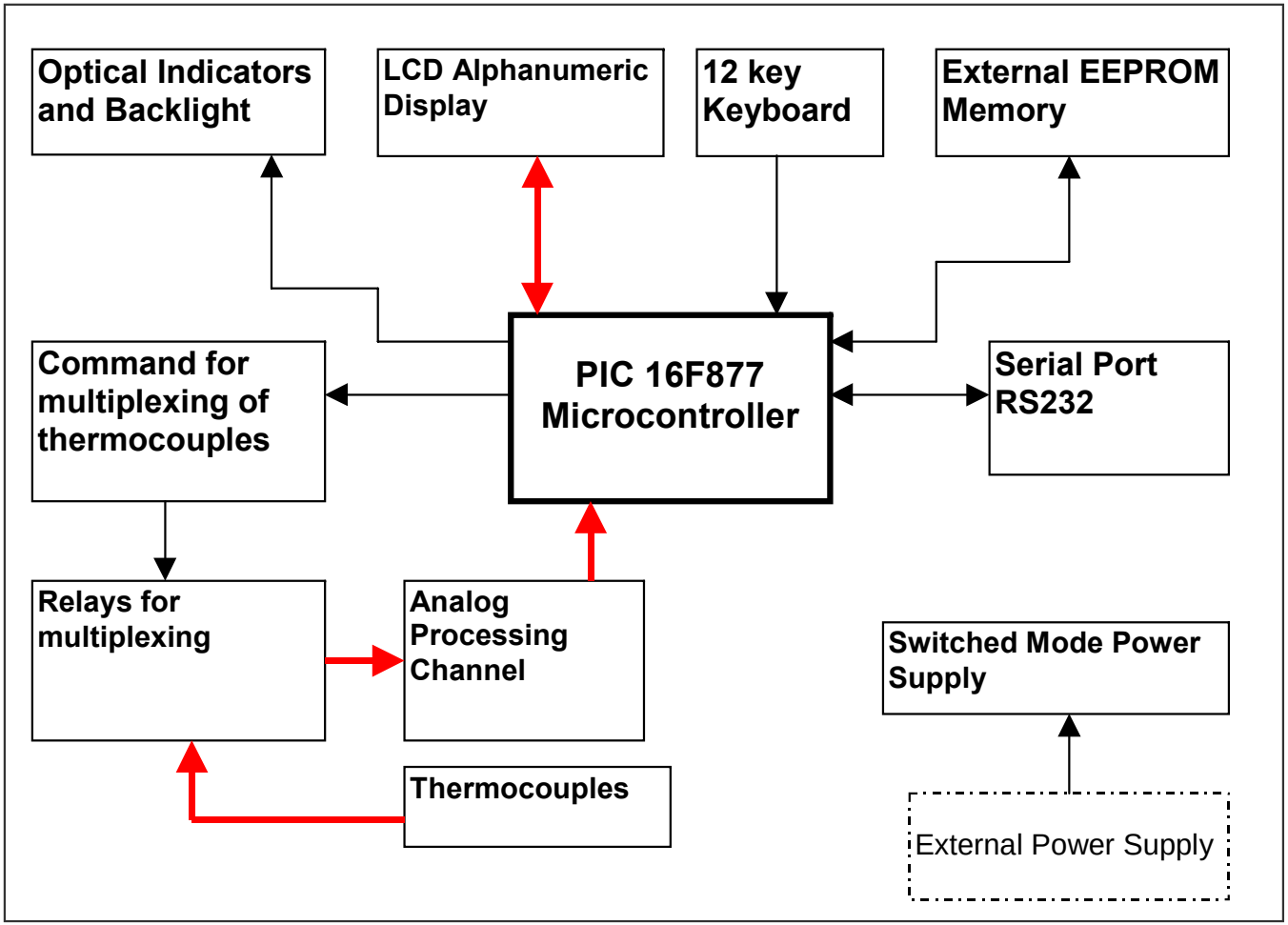
- **The system POLITEMP II uses thermocouples and is primary destined for temperature measurements of a reflow oven.**

- **It uses 8 measurement channels and is calibrated for K type thermocouple. For cold junction compensation an absolute temperature sensor is used (LM 35).**

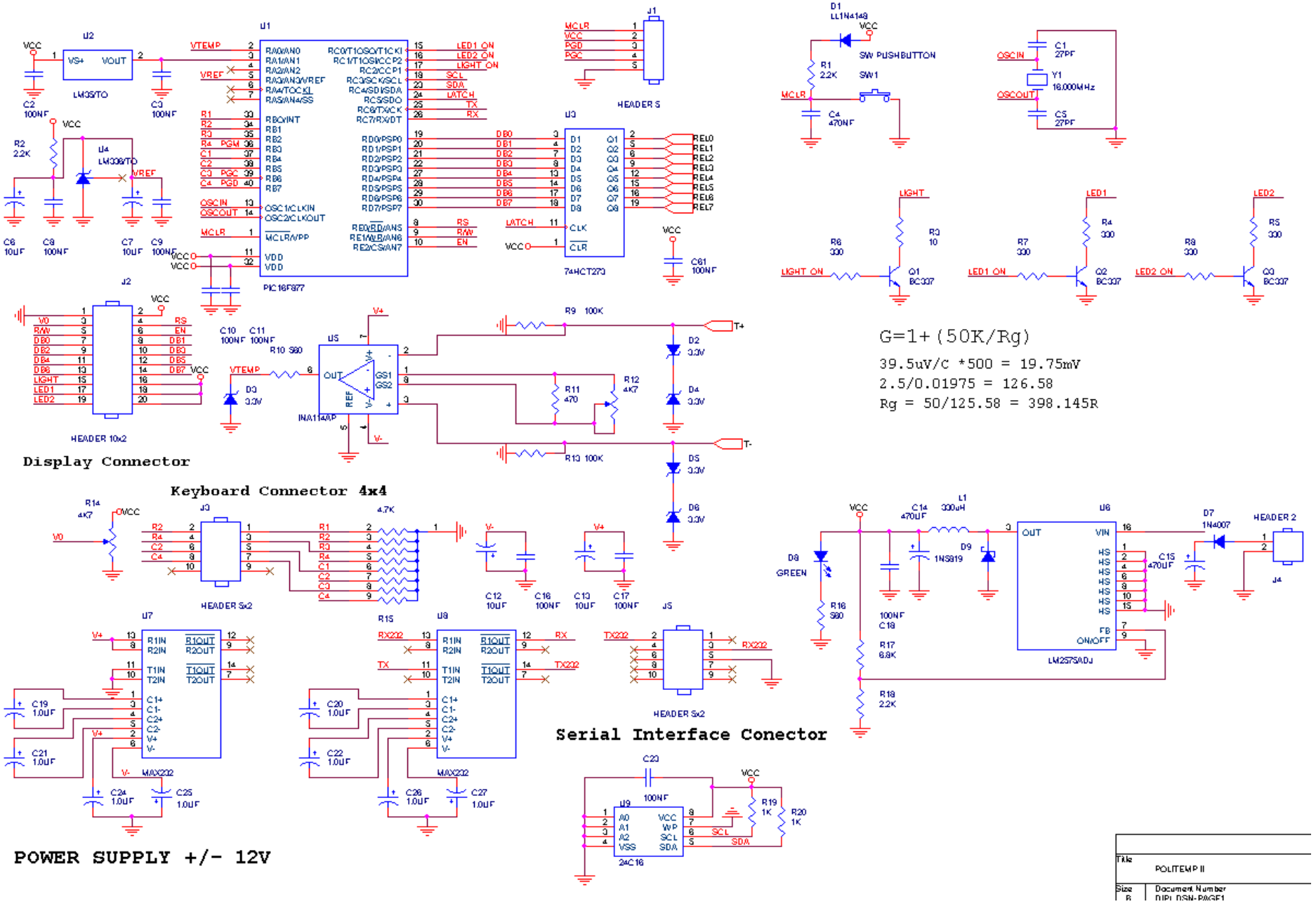
- **Can be used in data acquisition mode, connected to a PC or „stand alone" as a portable „data logger". In this last case the data are subsequently downloaded to a PC.**


POLITEMP II
Echipament de masura destinat
managementului termic al modulelor electronice
1 2 3
4 5 6
7 8 9
* 0 #
Proiect de diploma al studentului:
Bogdan - Alexandru ROSU
Iunie 2004

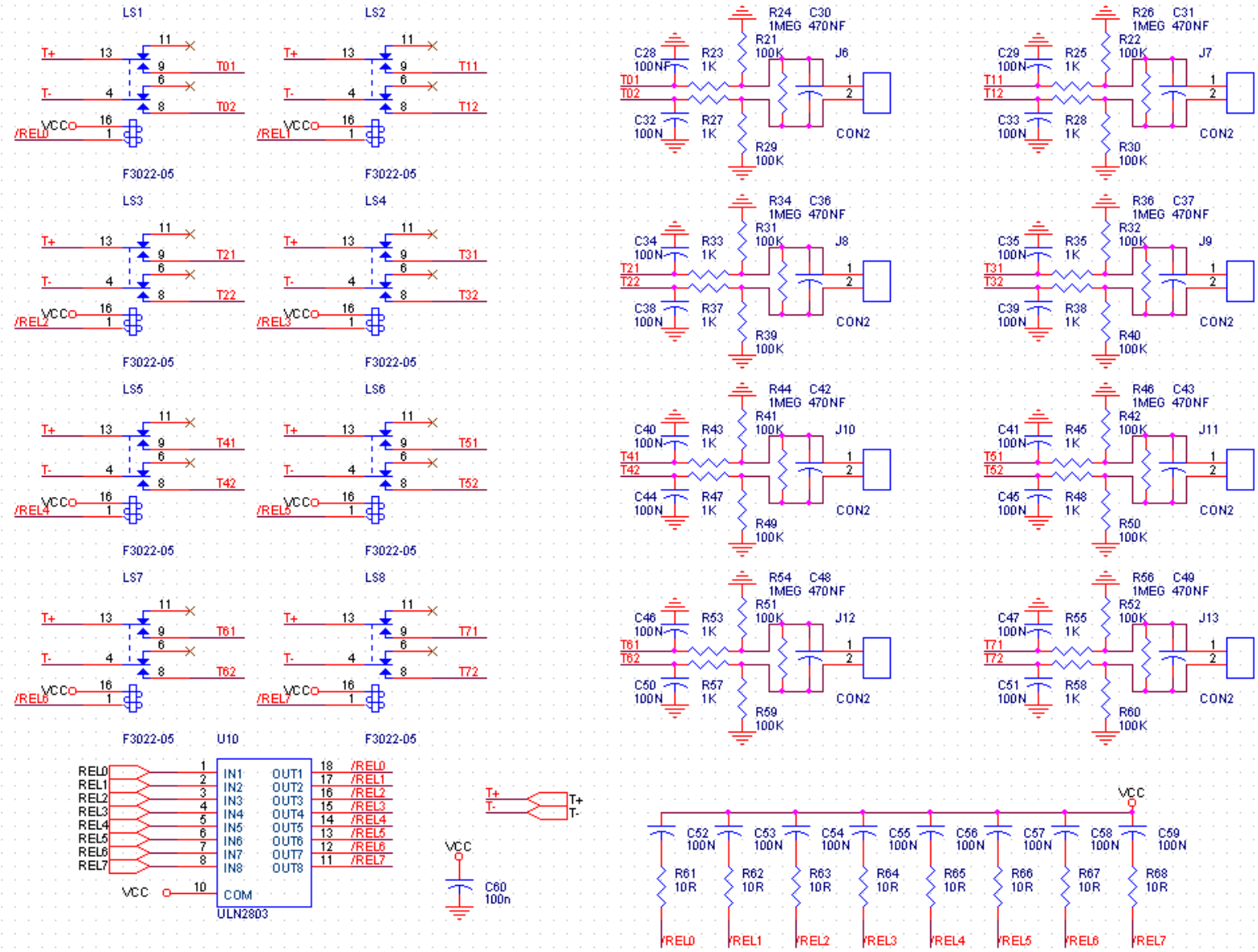

POLITEMP II
*Ies. 1-8sel ter
Term. 4 24.5C
Echipament de masura destinat
managementului termic al modulelor electronice
1
2
3
4
5
6



Block Diagram of Politemp II Acquisition System

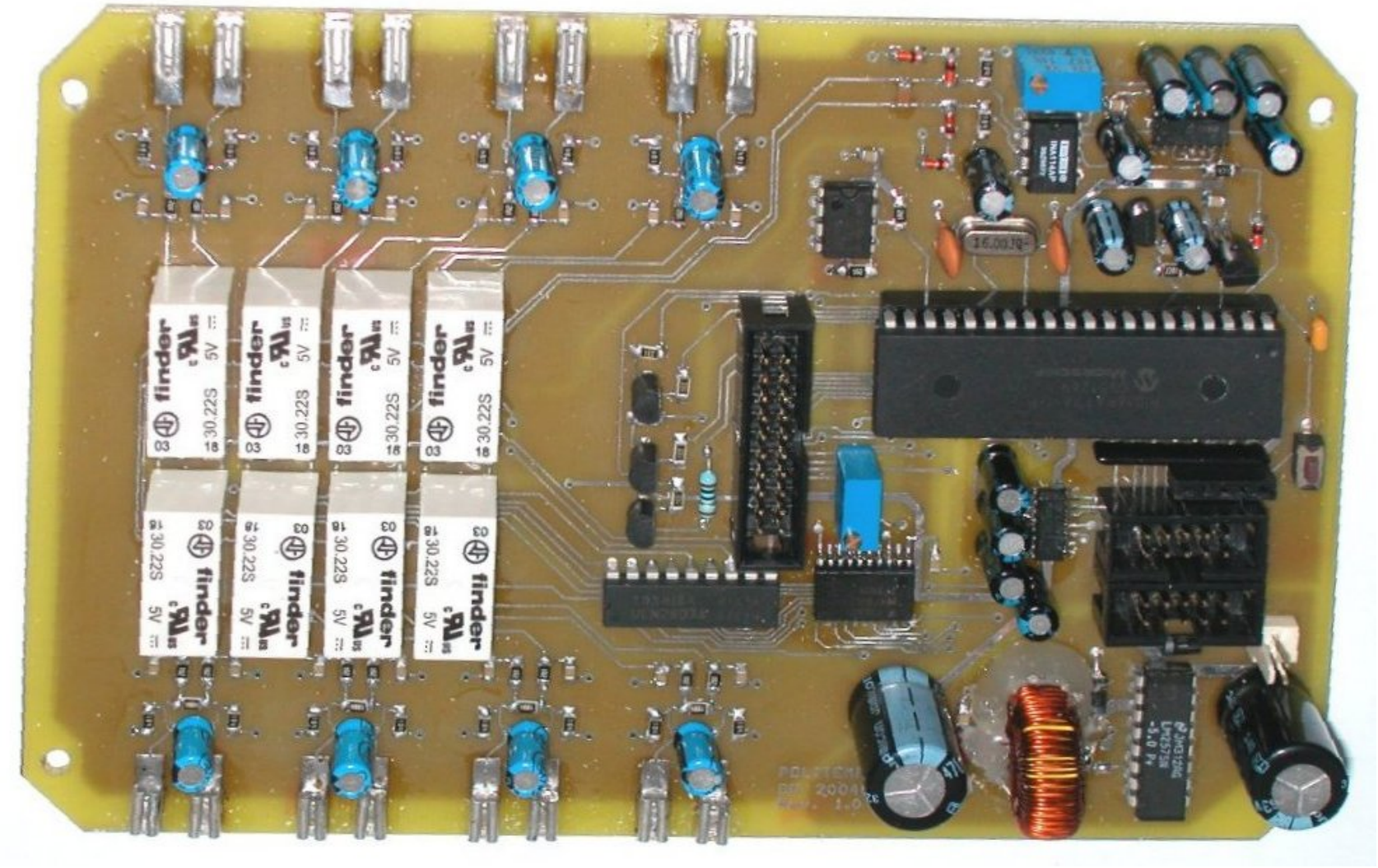


Schematic Page 1 of Politemp II

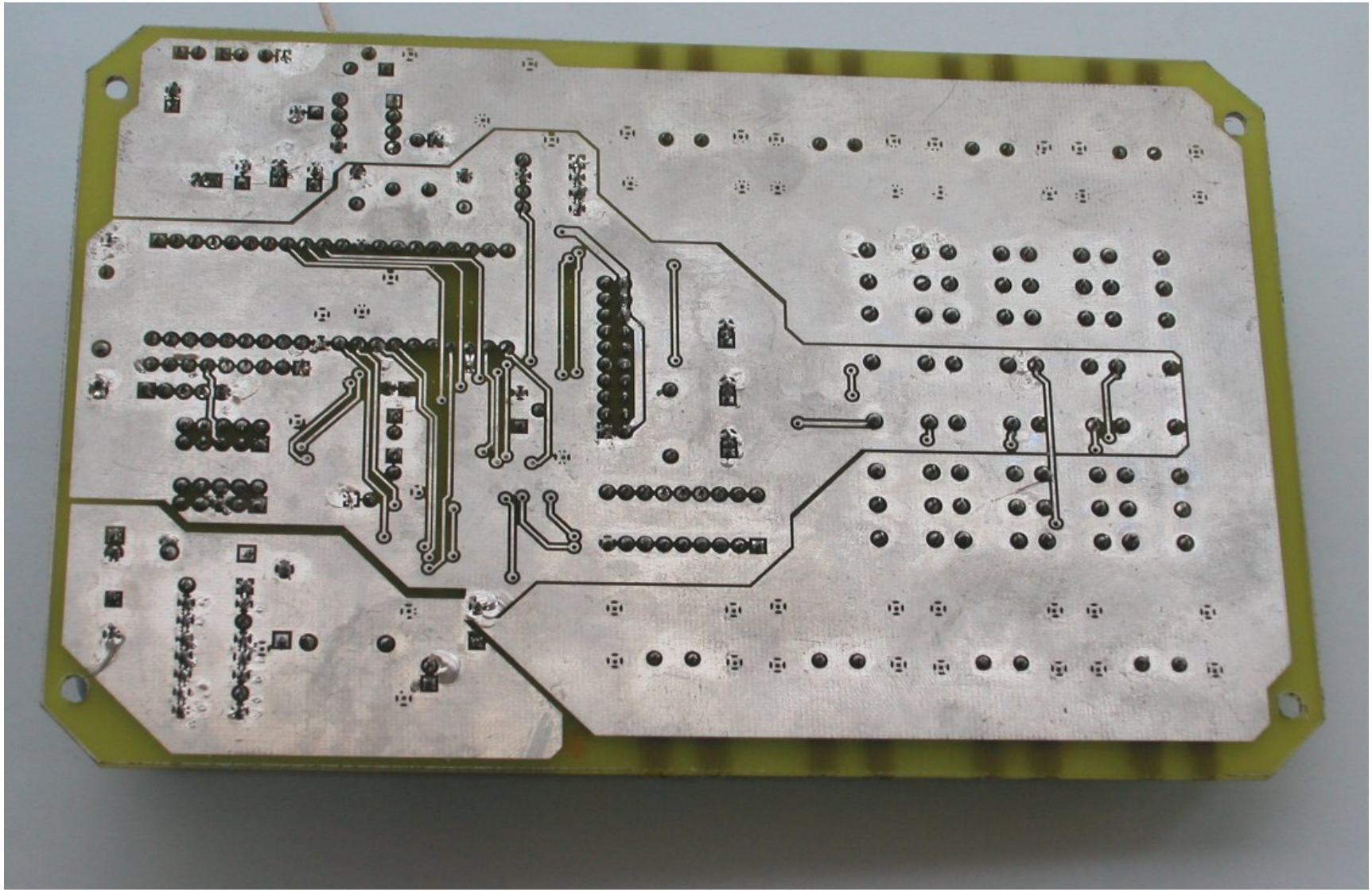


Schematic Page 2 of Politemp II

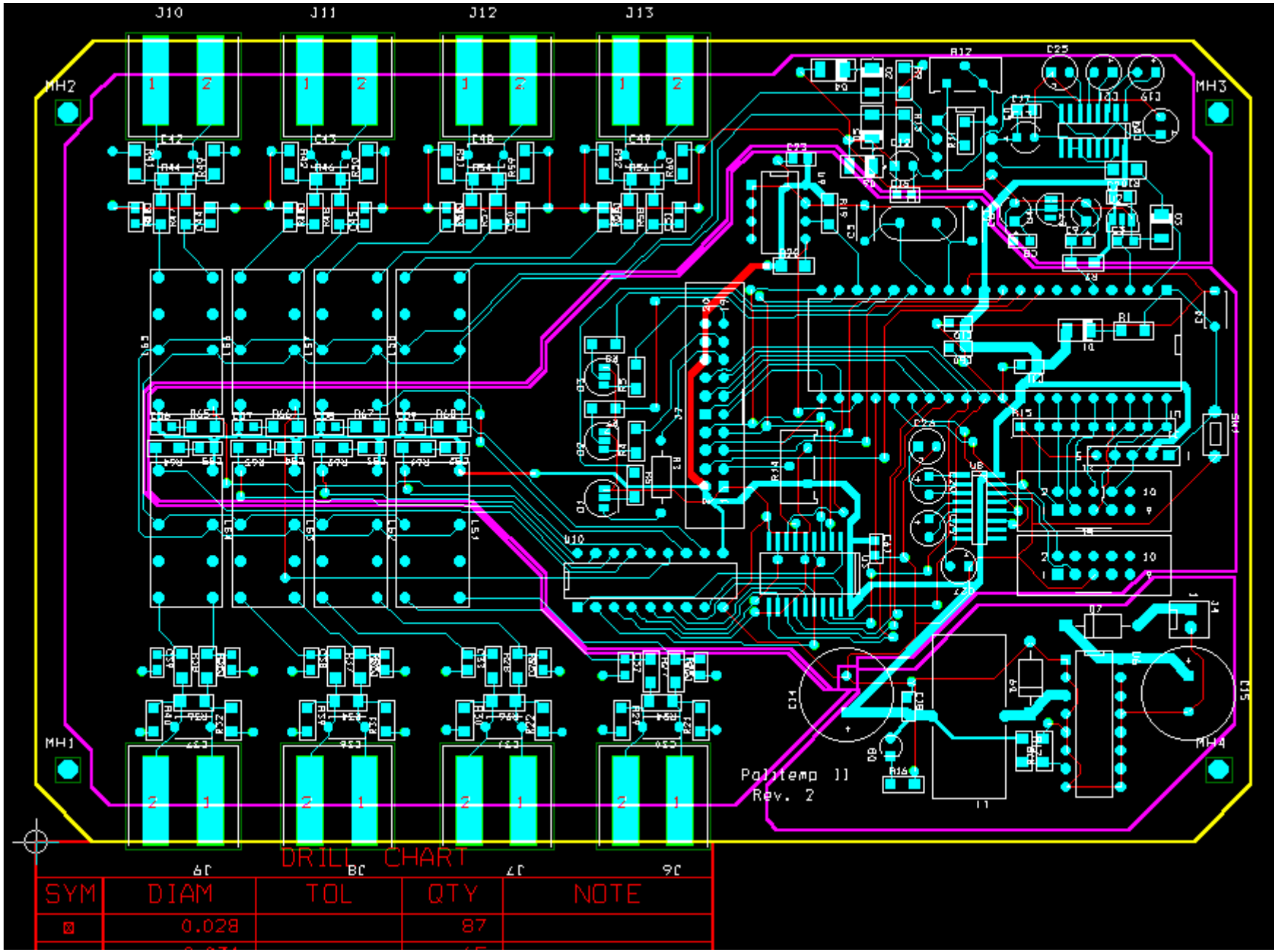

ECO.12150.06.SP
04/13
M5020PBF0020
finder



Top view of the main PCB assembly



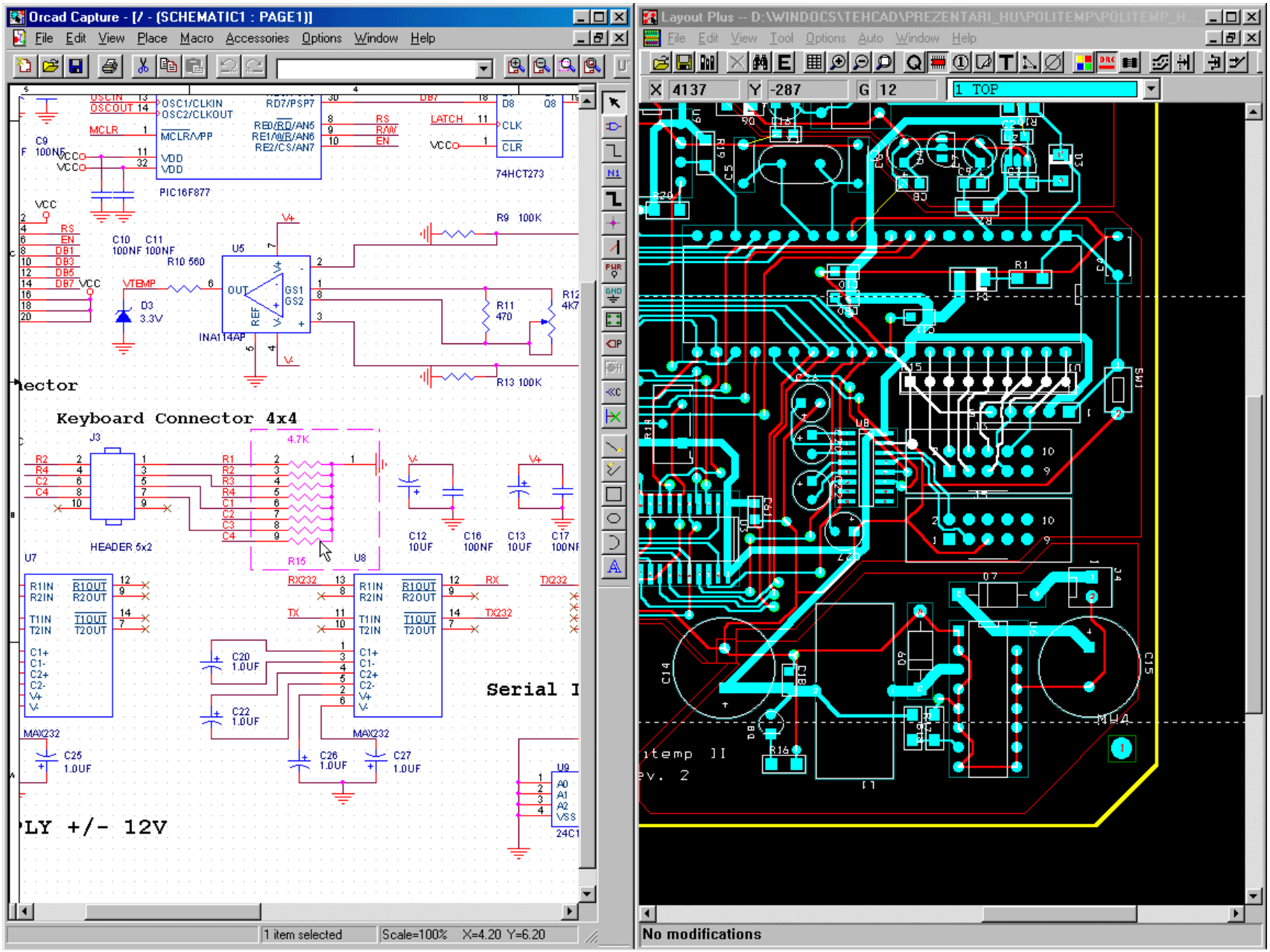
Picture of the bottom side of the main PCB



Shot of the design screen in Layout

Special Orcad techniques used in design:

- **Intertool Communication (Cross Probing)**
- **Copper Pour**
- **Copy tracks**

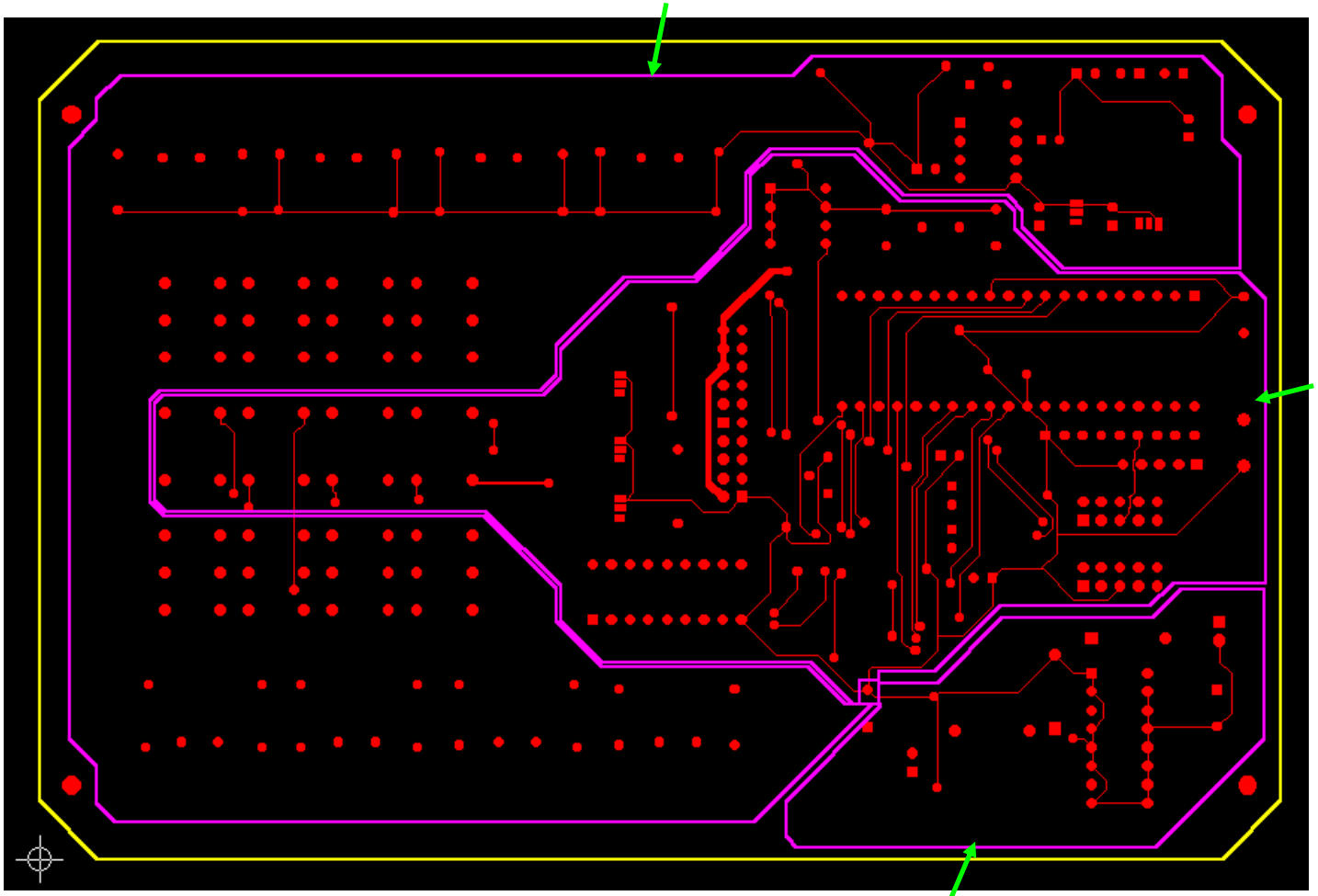


Cross Probing between Capture and Layout is very useful for complex projects, especially for component placement

Copper Pour

- Power planes are required for better decoupling of digital circuits, shielding or are required by thermal reasons.
- Usually the power planes are connected to ground.
- In complex modules using mixed analog-digital processing, there exists more "grounds" that are connected together, usually at one point.
- Orcad has the possibility to realize the so called "Split Power Planes".
- In our example there is a different situation: There is only one ground called "GND" and the planes are manually created.
- The common point is the negative pole of the filter capacitor.

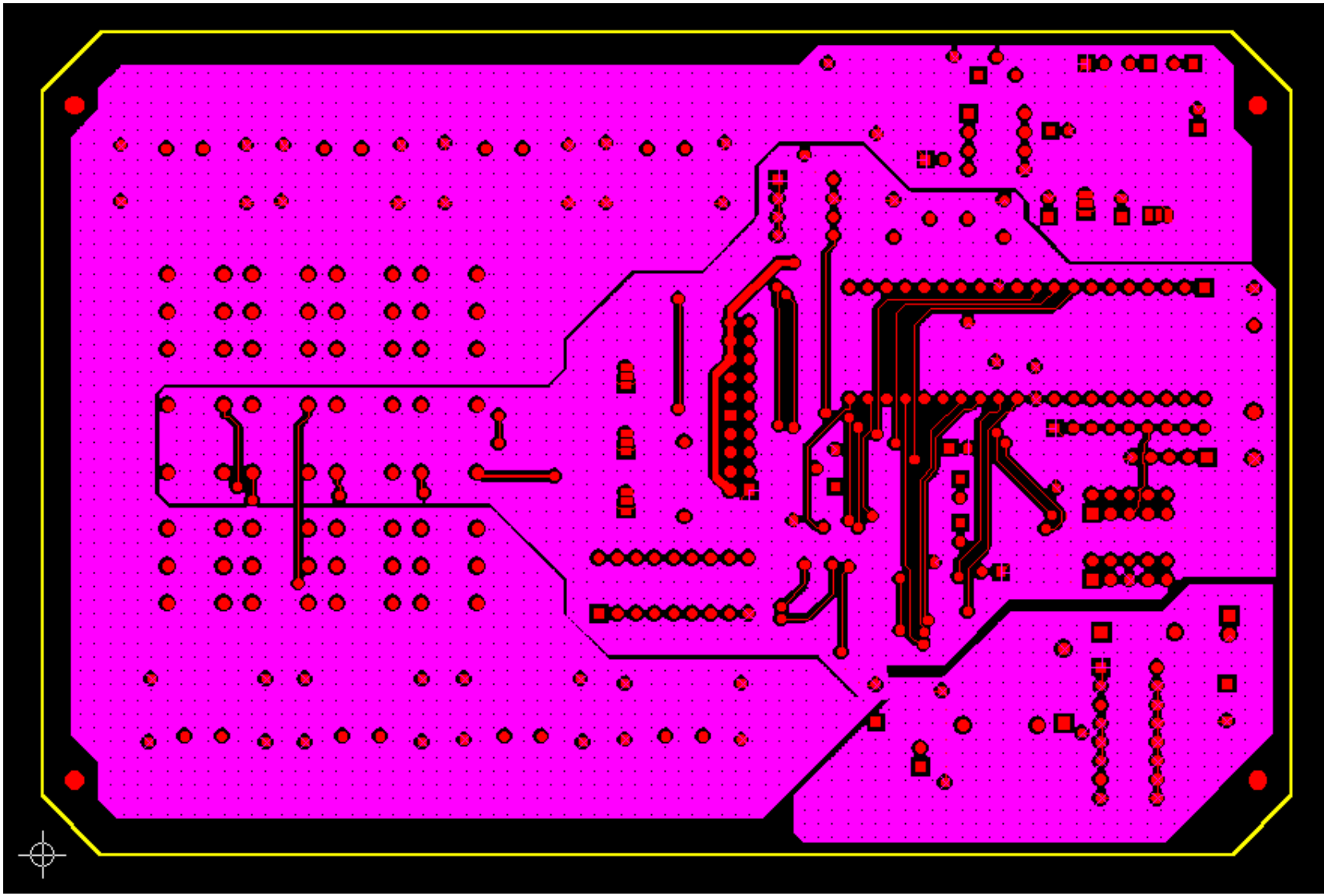
Obstacle 1- “Analog” Ground



Obstacle 2- “Digital” Ground

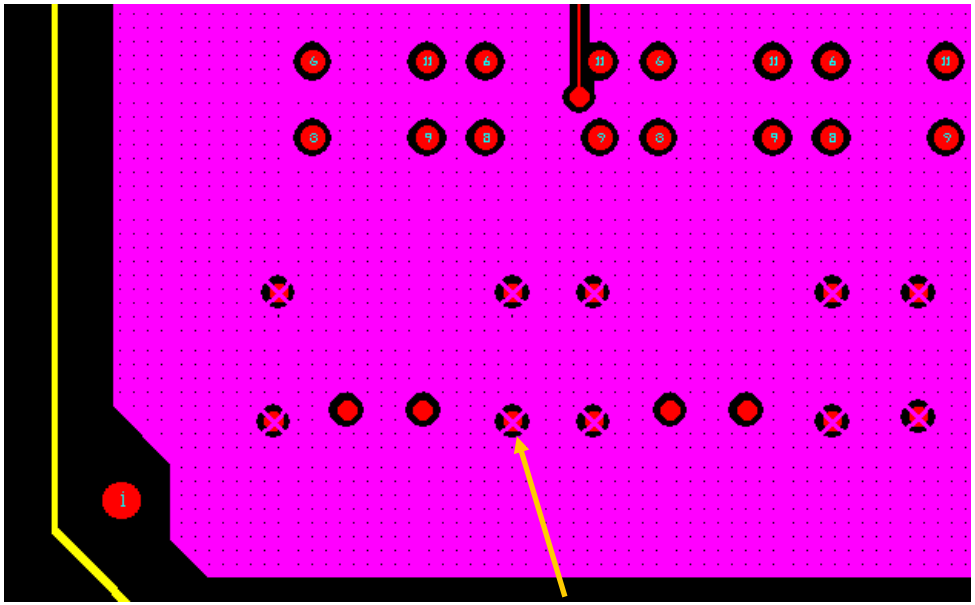
Obstacle 3- “Power” Ground

Bottom layer without Copper pour enabled- contour representation only



Bottom layer with Copper pour enabled

Copper Pour

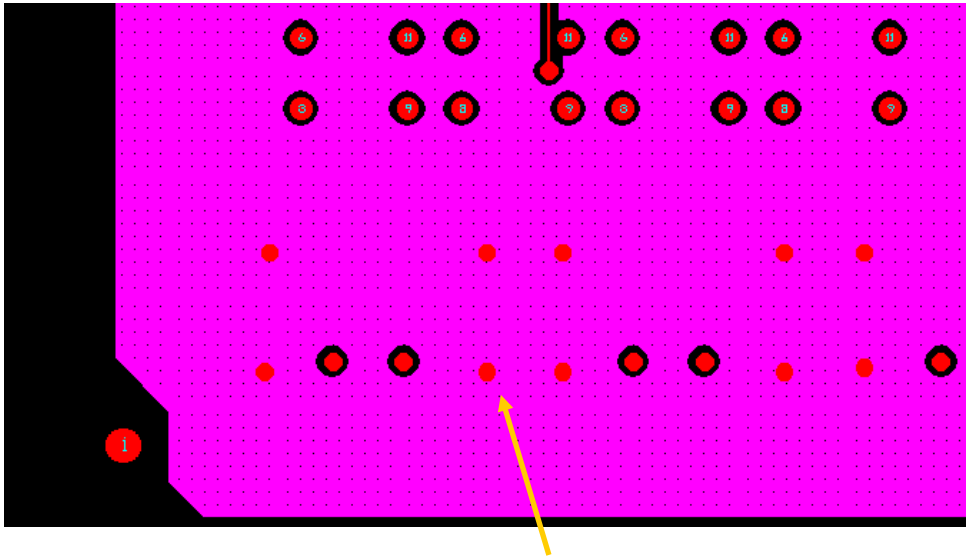


Thermal Relief

The connection of pads to the plane is controlled by the line:

THERMAL_COPPER_POUR_VIAS=YES

from LAYOUT.INI file



No Thermal Relief, pads are “flooded” in surrounding copper

To create Copper Pour areas:

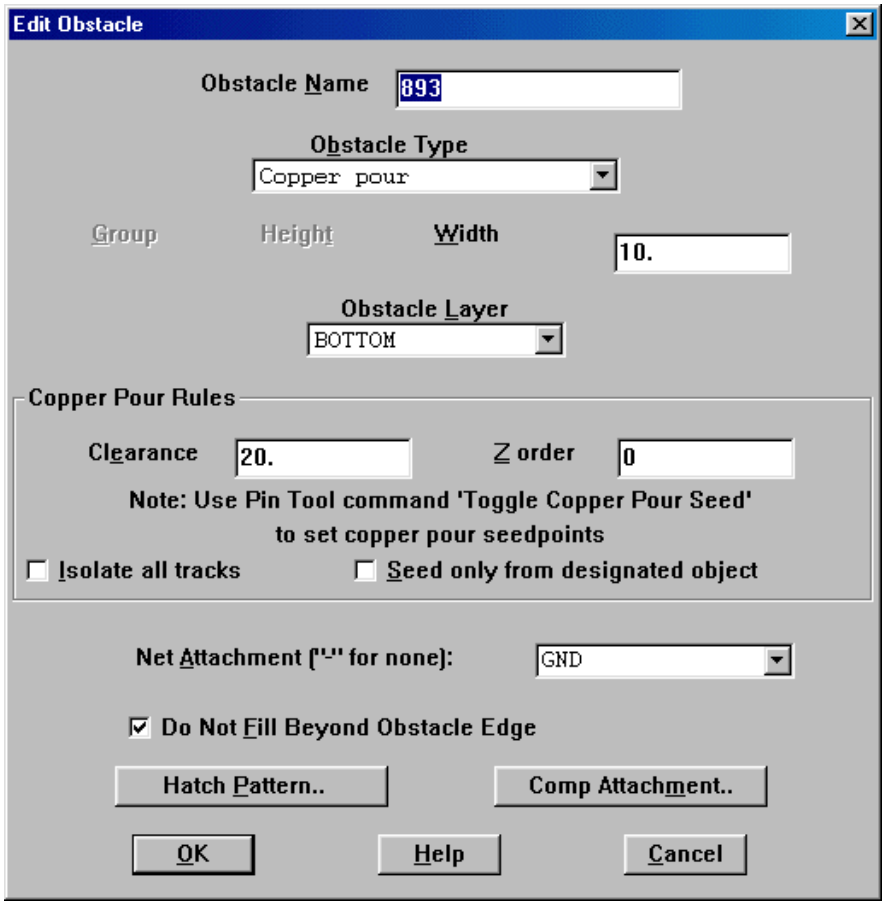
1. Create an obstacle (contour) of type “Copper pour”

   Select Layer

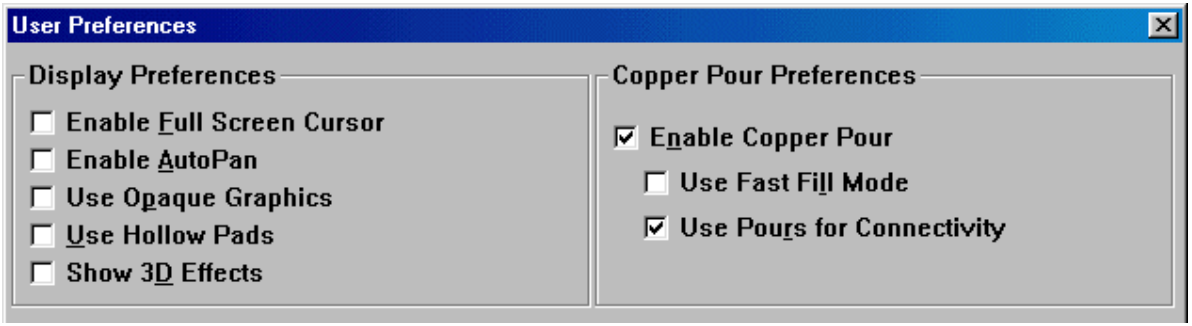
   Width

   Clearance

   Net Attachment



2. Activate the copper pouring from User Preferences menu



Copying Tracks

In some designs there are blocks (part) of circuit that are identical.

E.g. from our example the 8 processing channels for the thermocouples.

A good idea is to route one circuit and to copy the route pattern for the rest. This will save time and on the other hand a good similarity between the 8 channels is assured.

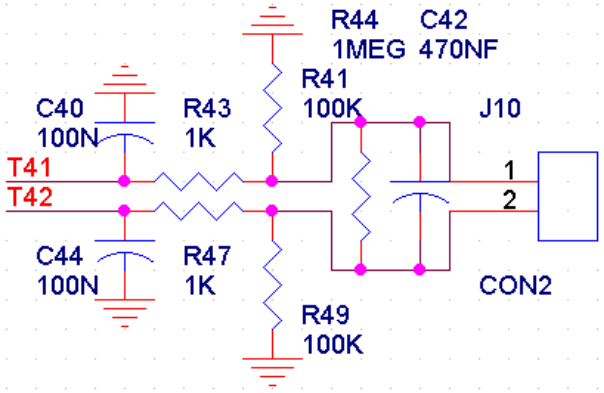
Many users claim the lack of ability to multiply the routing pattern.

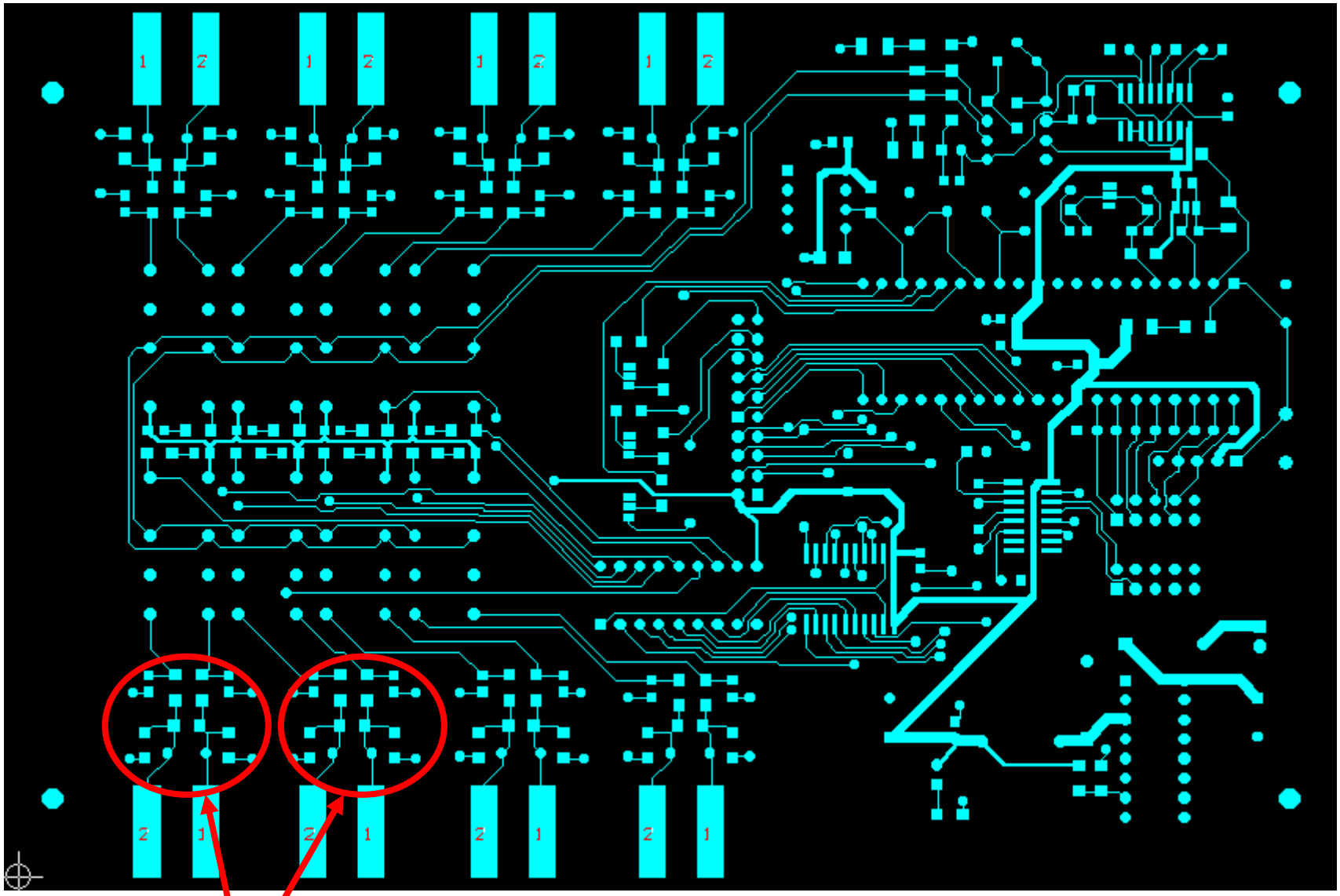
Solution: Using of CAM programs and editing of Gerber files.

Drawback: No backannotation is possible and errors can appear.

Orcad version 10 comes with the concept of "Design Reuse". The schematic must be initially prepared for that. Each reused block must be drawn in an hierarchical block and other special preparation are required for Netlist import. In the end, in Layout: Auto→Design Reuse.

Orcad version 9 has the Copy Tracks feature.



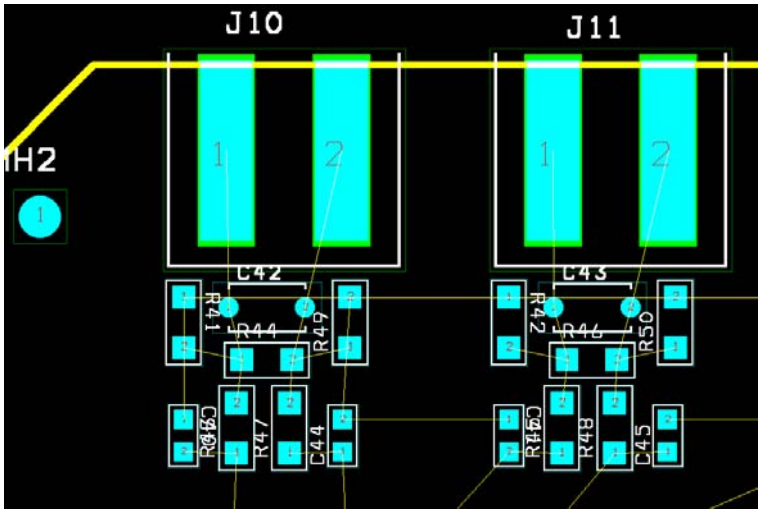


The tracks follow
the same pattern

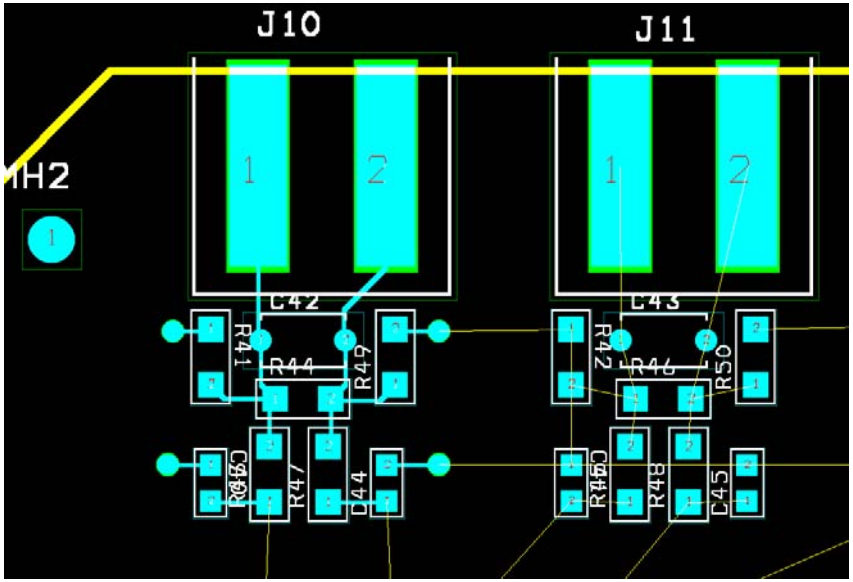
Top layer as displayed in Layout

To copy tracks:

1. Place the similar parts of the circuit at exactly the same relative distances. (How?)



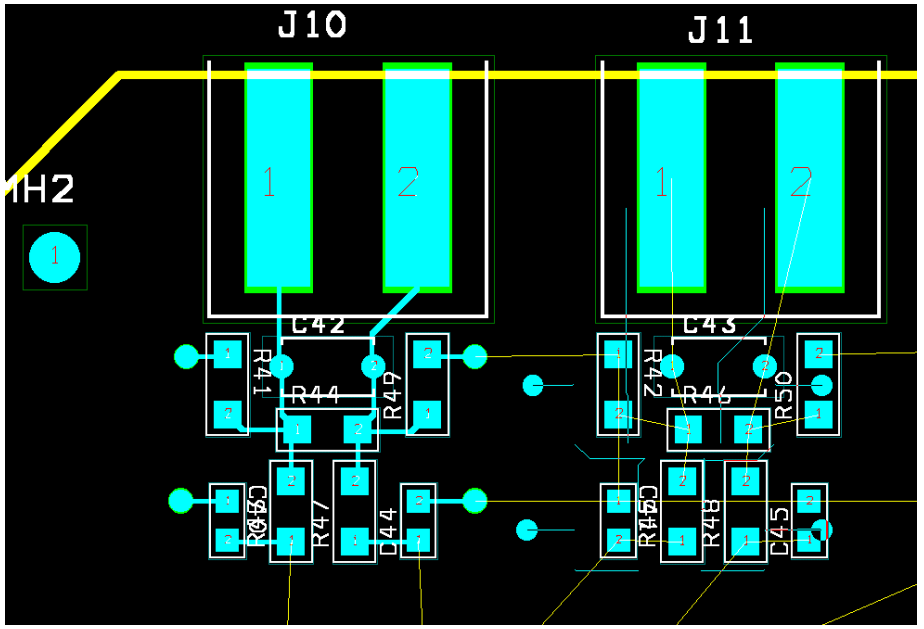
2. Route the first “Master” pattern that will be copied.



To copy tracks (next):

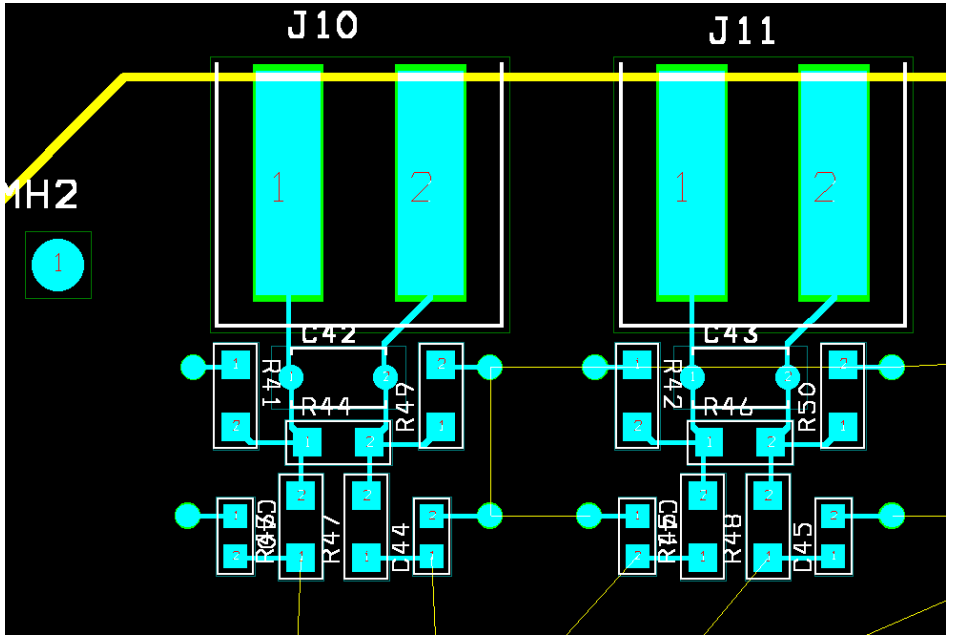
3. Frame select the tracks using one of the routing tools and use CTRL+C or INSERT key to make a copy of the tracks.

The tracks are moving together with the cursor.



4. Stop the cursor where the track segments fit and do “click”. The tracks are copied and the result is an identical track pattern.

Connections corresponding to tracks must already exists. If the placement is different or connections are not present the operation fails.



NATIONAL STUDENT CONTEST

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INTERCONNECTION TECHNOLOGIES IN ELECTRONICS (TIE)

Concursul TEHNICI DE INTERCONECTARE IN ELECTRONICA (TIE) este un concurs profesional studentesc ce are drept obiectiv proiectarea tehnologica asistata de calculator (CAE-CAD-CAM) a modulelor electronice.

http://www.tie.ro

Concursul reuneste studenti din mai multe centre universitare si este deschis tuturor studentilor pasionati de domeniu. Prin modul de organizare si corectarea publica a lucrarilor concursul isi propune sa promoveze spiritul de competivitate si profesionalism in randul studentilor interesati de packaging-ul electronic

- **TIE 2007 a avut loc in intervalul martie-aprilie 2007, fazele locale avand loc in fiecare centru universitar pe parcursul lunii martie 2007. Faza finala, la care au participat primii clasati ai fazelor locale, s-a desfasurat in perioada 12-14 aprilie 2007, la Suceava.**

- **La concurs au participat studenti, indiferent de facultate, care au cunoscut programe de proiectare asistata de calculator in domeniu, cu licenta. Pentru detalii suplimentare poate fi contactat directorul concursului, conf. dr. ing. Norocel Codreanu (norocel.codreanu@cetti.ro).**

UNIVERSITATEA "ŞTEFAN CEL MARE" DIN SUCEAVA
Facultatea de Inginerie Electrică şi Ştiinţa Calculatoarelor
Centrul de Cercetare în Sisteme de Control al Proceselor

UNIVERSITATEA "POLITEHNICA" DIN BUCUREŞTI
Facultatea de Electronică, Telecomunicaţii şi Tehnologia Informaţiei
Centrul de Electronică Tehnologică şi Tehnici de Interconectare

20 07

Concursul studenţesc
Tehnici de interconectare în electronică

TEHNICI DE INTERCONECTARE ÎN ELECTRONICĂ

Concurs profesional studenţesc
Faza naţională, Ediţia a XVI-a
Suceava, 12-14 Aprilie 2007

Concursul vizează verificarea cunoştinţelor concurenţilor în domeniul proiectării asistate de calculator a modulelor electronice.

Prin modul de organizare şi corectarea publică a lucrărilor, concursul îşi propune să promoveze spiritul de competitivitate şi profesionalism în rândul studenţilor interesaţi de packaging-ul în electronică.

Participă studenţi din centrele universitare:

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